RABBLE 65

TECHNICAL MANUAL

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RABBLE 65

HARDWARE MANUAL

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INTRODUCTION

The information contained in this manual outlines procedures to be followed in unpacking, assembling and operating your Rabble 65 microcomputer system. Please follow these instructions carefully. Preferably, you should pour yourself a long cup of coffee and read the manual completely before unpacking any of the components. This will ensure a better understanding of the system during assembly with a minimum of problems.

UNPACKING

Carefully remove the system components from their packages and save all packaging materials. They may be required later to return damaged or faulty components. Ensure that all components ordered are accounted for. Any deficiences or breakages should be referred immediately to your supplier.

DESCRIPTION

The Rabble 65 microcomputer, by Rabble Ozi Computers, has been designed and manufactured in Australia. It is a fully expandable system capable of rivalling any other system currently on the market. The Rabble 65 has been designed as a single board system with a seperate and easily relocatable keyboard. The overall size of the main printed circuit board is 370 mm x 320 mm

A full size keyboard is provided to ensure compatability with most operating systems. The full upper and lower case character set is available. The Rabble 65 keyboard is a software scanned or polled keyboard, which offers greater flexibility to the user in designing application software.

The video display is generated by a Cathode Ray Tube Controller chip, the MC 6845. This is configured to provide a display format of 25 rows of 80 characters. The CRTC is supported by a character generator providing 256 characters, which include all ASCII characters as well as numerous games, symbols and elements. These provide sufficient variety to be able to construct chess board pieces or even space ships and tanks.

The video output is a composite video signal suitable for coupling directly to a video monitor via an RCA connector. A monitor is recommended to ensure the resolution that the Rabble 65 is capable of providing. Lesser quality will be experienced with modified TV sets.

The Rabble 65 will support, contiguously, up to 48K of CMOS RAM and a further 4K of CMOS RAM is provided for on the board. 2K of the latter RAM is for the video display and the other 2K for user/system RAM which

is cold start protected from BASIC. You can place your special user routines here without overwriting them with BASIC. The CMOS RAM is located at the following locations:-

DECIMAL	HEX	
0 - 49151	0000 - BFFF	48K contiguous RAM in 2K blocks
51200 - 53247	C800 - CFFF	2K system/user RAM
53248 - 55295	D000 - D7FF	2K video RAM
57344 - 61439	E000 - EFFF	Optional user ROM
61440 - 65535	F000 - FFFF	System Monitor ROM (RA-65)

A total of 56K of ROM is provided for on the Rabble 65. The RA-65 monitor is provided with all systems and provides the user all the facilities required to operate and write machine code programmes, as well as to provide the disk system boot functions. This system monitor is detailed explicitly in the System Software Manual. The 56K ROM is acheived by paging the memory block from $8000 - BFFF in three pages, and selecting an 8K block from $E000 - FFFF. A fourth block of 16K is made available for RAM. The paging is discussed in more detail in chapter 12.

A host of peripheral devices are supported by the Rabble 65. The first of these is the Floppy Disk Controller, which can operate up to four disk drives. These drives can be 5 1/4" or 8", single sided or double sided with AC or DC driven motors. An on board data separator is provided for as well as a motor control for DC driven drive motors. The Rabble 65 is Ohio Scientific compatible and will boot up their popular software packages 65DV3.2, 65DV3.3, and many others with minimal modification. Refer to the System Software Manual for details on these.

Other I/O support includes an on board RS232 port with a selectable baud rate generator and a casette port which will operate with a standard low cost domestic casette recorder. Two expansion busses are provided for. A 16/18 pin I/O Buss provides a fully decoded port system to drive up to eight ACIA's (serial I/O ports) or a number of other directly accessable I/O devices. These devices are not provided on board but are available separately. 16/18 pin expansion devices available, or soon to be released, include a High Resolution colour graphics board, an EPROM programmer, programmable sound generators, voice recognition, Votrax SC01 speech generator, prototype breadboard, and many others. The second buss system is a 50 way buss which provides full access to the microcomputers control and data buss, permitting expansion to occupy the total available memory, or for multiprocessor operation.

The heart of this Rabble 65 is controlled by a CPU chip manufactured by a number of sources and numbered "6502", later versions will employ an updated version of this chip manufactured by Rockwell, the "65C02".

This manual does not give programming details to the user on any of the languages mentioned. Anyone wishing to become proficient in programming in any of the high level languages or in machine code are advised to purchase a book on that language which is available from many bookshops and written by numerous people. However, many of the words

contained in the manual, which may be new to you, are explained in the Glossary elsewhere in this manual.

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MEMORY MAP

```
FFFF

          System Monitor RA65 8K ROM

E000
DFFF
          Not allocated.
D800
D7FF
          Video Display Memory
D000
CFFF
          2K CMOS RAM
C800
C7FF
          System Input Output


          C73x  18 pin buss number 4
          C72x  18 pin buss number 3
          C71x  18 pin buss number 2
          C70x  18 pin buss number 1
          C4xx  6532 RIOT keyboard control
          C06x  6522 VIA keyboard and auxillary system control
          C01C-F  6845 CRTC video controller
          C010-3  6850 FDC ACIA
          C000-3  6821 FDC PIA

C000
BFFF      System one          System two          System three
          Top of 48K RAM      Top of 8K ROM       Top of 16K ROM
                              3 pages             3 pages

A000                          Start 8K ROM pages
9FFF                          Top of 40K RAM

8000                                              Start 16K ROM pages
7FFF      Top of 32K RAM


3FFF      Top of 16K RAM


01FF
          Stack
0100
00FF
          Page Zero
0000
```

CHAPTER 2

PARTS LIST

Integrated Circuits

Type	Qty.	Socket No.	
74LS00	9	49,53,65,83,99,105,106,111,113.	
74LS02	2	84,92.	
74LS04	8	4,7,45,47,51,59,88.	
7406	1	117.	
74LS08	3	9,26,43.	
7416	1	81.	
7417	5	78,79,89,91,101.	
74LS20	1	48.	
74LS27	1	52.	
74LS30	1	75.	
74LS32	2	3,28.	
74LS74	4	82,103,104,110.	
74LS76	1	76.	
74LS123	4	63,95,98,100.	
74LS138	8	1,2,6,8,46,50,66,67.	
74LS139	3	27,68,90.	
74LS145	1	29.	
74LS157	3	54,55,56.	
74LS163	1	58.	
74166	1	69.	
74LS175	2	85,86.	
74LS245	3	44,73,87.	
74LS367	3	60,61,62.	
74LS374	1	71.	
74LS393	2	74,112.	
NE556	1	116.	
DM8602	1	102.	
CD4040	1	96.	
CD4051	1	97.	
CA3130	1	64.	
MC1488	1	93.	
MC1489	1	94.	
2764	1	10.	System Monitor.
2732	1	70.	Character Generator.
2764	3	11,12,13.	System Languages.
6116LP3	26	14-25,30-42,72.	CMOS RAM.
6502	1	77.	CPU.
6522	1	107.	VIA.
6532	1	108.	RIOT.
6821	2	80,109.	PIA.
6845	1	57.	CRTC.

6850	2	114,115.	ACIA.

IC Sockets

8 PIN	1
14 PIN	44
16 PIN	30
18 PIN	4
20 PIN	4
24 PIN	29
28 PIN	4
40 PIN	6

Resistors 5% 0.25W

47	3	
100	1	
150	1	
390	2	
1K	9	
2.2K	4	
3.3K	3	
5.6K	2	
10K	2	
15K	1	
100K	1	
470K	2	
470 x 9	3	Bourns 4310R-101 Resistor SIP
10k	7	Cermet trimpot VTP Linear

Capacitors

68pf	1	630V ceramic subminiature
100pf	1	630V ceramic subminiature
150pf	2	630V ceramic subminiature
220pf	1	630V ceramic subminiature
1nf	6	100V polyester film
100nf	20	100V polyester film
1uf	1	35V Tantalum
10uf	20	25V Tantalum

Miscellaneous

IN914	3	Diodes
Pushbutton	1	SPST PC mounting
Crystal	1	16MHz

Connectors

50 way	2	~~shielded~~ SHROUDED DIP headers
36 way	1	~~shielded~~ DIP headers
20 way	2	~~shielded~~ DIP headers

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DB25PSAA 1 RS232

CHAPTER 3

GENERAL ASSEMBLY INSTRUCTIONS

This board has a very high density of packages and trackwork. For this reason it is not recommended for beginners to cut their teeth on. Warranty claims for damage caused by poor user workmanship will not be honoured. Experienced kit builders will require the following tools to assemble the Rabble 65 successfully:-

Temperature controlled soldering iron with a tip diameter of 2.4mm or less

A cloth or wiping sponge to keep the tip clean

A desoldering tool or solder wick

1.25mm or 0.71mm 60/40 resin core solder

Small pair of diagonal cutters and long nose pliers

Test equipment should consist of a multimeter, oscilloscope, frequency counter and logic probe.

Before starting assembly, check the board carefully for any shorted, open circuit or damaged tracks. All care is taken in the production of these boards. Any faults can be repaired before construction or returned for replacement.

Fit and solder IC sockets to the board first. We recommend the use of sockets wherever possible, as servicing at a later date becomes a much simpler task. Solder each pin of each IC socket only on the underside of the board, as the holes are plated through the board, making connection with the other side. Do not miss pins because of an apparent pad with no tracks radiating, a track will most likely be attached on the top side of the board. Follow this with the fitting of all resistors, capacitors, resistor packages and other discrete components, including peripheral sockets.

It is recommended that all discrete components and sockets be fitted at this stage to provide for each upgrading of the Rabble 65 at a later time, by simply plugging in chips.

After all components have been soldered into position, inspect each solder joint carefully to ensure no dry joints exist. Check also for solder slivers which may cause problems and remove, solder blobs covering more than one pin of an IC are also a hazard to beware of.

Any resin deposits on the board can be cleaned off at this stage by wiping the affected spots with a cotton bud dipped in methylated spirits.

When satisfied that all the above is of a high standard, you can mount the keyboard. This is not an easy task as there are over 100 pins to be fitted into over 100 holes at once, without missing any. First ensure that all pins on the base of the keyboard are erect, after removing the foam packing from the bottom. If any are not erect, carefully bend them until they are. It is best to lay the keyboard on a soft but firm surface with the key tops down and the space bar facing you. Turn the keyboard PCB over and carefully align the holes over the keyboard pins and fit the keyboard. Force should not be used in this operation. When the board is fully seated over the keyboard, solder two terminals, one at each end of the keyboard, to hold things in place and check that all pins of the keyboard have been fed through the board. If not, untack the keyboard, clean the plated through holes, repair the keyboard and try again. When fitted correctly, solder all connections on the keyboard then check and clean if necessary.

To facilitate the ease of construction, the rest of the assembly instructions will be described in logical sub-assemblies, where a circuit description will be given at the same location. We believe that this will provide an easier to follow method of assembly as well as giving a better understanding of how the computer operates.

The description will be broken up into 16 parts to describe the eleven major sections of the computers main board. These major sections are:-

1 Chapter 4 Power Supply

2 Chapter 5 Keyboard, and system VIA, and RIOT - - - - 2 parts

3 Chapter 6 Video display controller - - - - 2 parts

4 Chapter 7 Serial I/O

5 Chapter 8 Centronics port

6 Chapter 9 Floppy disk controller - - - - 2 parts

7 Chapter 10 16/18 pin I/O bus

8 Chapter 11 RAM - - - - 3 parts

9 Chapter 12 ROM

10 Chapter 13 CPU

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11 Chapter 14 I/O Decoding

Each major section of the computer description shows in detail the relevent section of the circuit and component layout. A full circuit description, together with setup and alignment instructions are included, as well as fault location details.

CHAPTER 4

POWER SUPPLY

The Rabble 65 power supply is a high voltage switch mode supply. It is provided as a sealed unit, which should be returned to your supplier for service if required. This style of power supply has been chosen for its high efficiency and reliability.

The efficiency of this type of power supply comes from the use of a high frequency switching oscillator, driving a ferrite core power transformer. The resultant low voltages are then rectified and because of the high frequency ripple, only a small amount of filtering is required.

Input voltage	240 VAC
Output voltages	+5.0 +12.0 -12.0 -5.0

The power supply is capable of operating the fully populated CPU board as well as two 5.25" floppy disk drives.

CIRCUIT DESCRIPTION

The AC voltage is fed via a mains filter into a bridge rectifier to provide a DC supply which is then capacitively filtered. This DC voltage drives an oscillator at a frequency of around 20KHz, this varies with actual load. The oscillator output is then fed to the ferrite core transformer, with it's many windings. The secondary outputs are then rectified in the normal manner to provide unregulated supply outputs which are filtered with electrolytic capacitors. The +5 volt output is fed to a voltage sensing network, which constantly monitors the output voltage, and when it rises above +5 volts it turns on a LED within an opto coupler. The transistor in the opto coupler then causes the oscillator to shut down and thus the secondary voltage starts to decrease. When the +5 volt supply starts to drop below +5 volts the LED turns off and the oscillator starts up again. As the +5 volt supply is controlled by the primary winding of the transformer, all secondary windings will be regulated simultaneously.

CAUTION

The Rabble 65 power supply contains high voltages within the case. Many of the components are at mains potential, and specialised equipment

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is required for servicing. There are no user adjustments inside. Should your power supply develop a fault, DO NOT OPEN OR ATTEMPT TO REPAIR. Send your power supply to your Rabble 65 dealer for service.

For 8" floppy disk drives, it is neccessary to provide an additional power supply to drive the solenoides and drive motor.

For a single 8" slimline drive in the standard Rabble 65 CPU case, a 24 volt supply at 1 Amp will be required. This supply is of conventional design, and fits into the CPU case with the floppy disk drive.

If twin 8" drives are being implemented, then a separate case is required to house these drives, for both slimline or standard size drives. The power supply for these drives will be fully self contained within the drive enclosure. It is of conventional design and delivers +5volts at 2 Amps and +24 volts at 2 Amps.

CHAPTER 5

KEYBOARD CONTROLLER

ASSEMBLY

The keyboard should already be mounted as detailed in the general assembly instructions. Fit 40 pin sockets for IC's 107 and 108, fit a 20 way DIP header to the CPU board just below IC 108. The other 20 way DIP header should be fitted to the keyboard assembly. Insert a 6522 into socket 107 and a 6532 into socket 108 to complete assembly.

CIRCUIT DESCRIPTION

The keyboard is encoded in a 12 x 8 matrix, of which not all combinations are used, to provide a comprehensive ASCII character set. The keyboard has its eight columns read by the system RIOT, IC 108, on port B and port A reads the first eight rows of characters needed by the keyboard. A further four rows of characters and control functions are input to the system VIA IC 107, port B bits 0 - 3.

The VIA, 6522 - IC 107, is located at $C060 (Port B I/O register) and the RIOT, 6532 - IC 108, registers at $C480 for port A and port B at $C482.

When any key is pressed, it connects one of the column lines at the RIOT, port B, to one of the row lines of the RIOT, port A or the VIA port B.

The monitor reads the keyboard by accessing each column in turn, then reading the row port to ascertain if a key has been pressed on that row, if not it checks the next row and so on. Once the key has been found, the monitor returns the ASCII value for use by the computer programme.

The 6532, RIOT, also contains 128 bytes of RAM located at $C400 - $C47F, decimal 50176 to 50303. This area of RAM is used by the system monitor for system control and operation and is not generally available for user software use.

DEBUGGING

The keyboard should be checked if only one character is not being received. The method of doing this is to turn the power off and remove IC's 107 and 108. Then locate the offending key on the keyboard circuit and find which port inputs refer to it, and measure the resistance whilst holding the key depressed. For example, key "1" is located at intersecting points of RIOT PB7 and PA3, corresponding to pins 16 and 11 of IC 108. Measure at this point and a closed circuit should appear with the switch pressed and an open circuit with the key released. For the space bar, the column is PB1, IC 108 pin 23 and the row is VIA, PB3, IC 107 pin 13. If it appears that the key is faulty, repeat the resistance check at the rear of the P.C.B. directly behind the suspect key. If this checks OK, then there is a faulty track. If the fault is still evident, remove the key cap carefully and check the alignment of the contacts, if necessary clean the contact by inserting a piece of thin card (a corner of a business card is ideal), between the contacts and gently wipe them without applying any side pressure.

If more than one key is defective, note down all the defective keys, and it will most probably be that they will all be related to one port line, refer to the keyboard circuit. Check the common line from the keyboard to the appropriate pin of the VIA or RIOT and repair if necessary. If this does not cure the defect, then it is probable that the VIA or RIOT is faulty and should be replaced, only if it appears that one port line is affected.

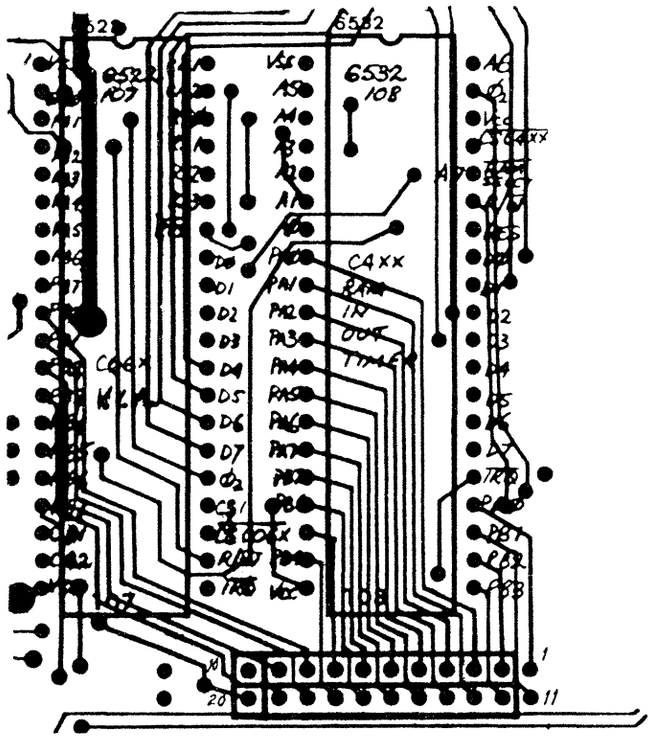
If the keyboard does not appear to function at all then check that the control lines to the VIA and RIOT are present.

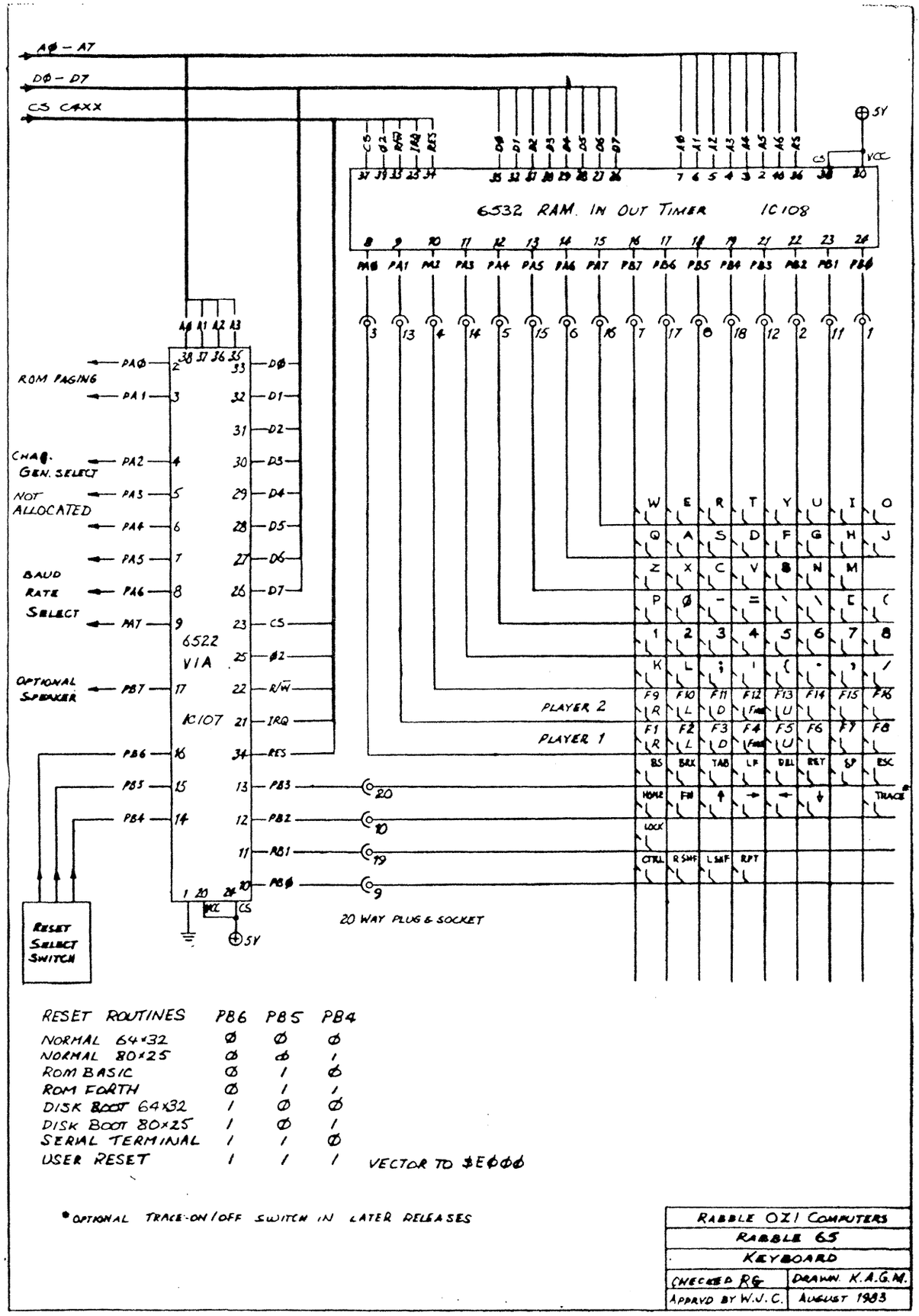
	RIOT	VIA
Phase two clock	pin 39	25
Register select	" 36	--
Read/write	" 35	22
Data lines D0-D7	pins 33-26	33-26
Address lines	" 7-2, 40	38-35
Chip select	" 37	23

Follow up any missing signals, and if all present, replace the RIOT first, then if necessary, the VIA.

THE KEYBOARD

The Rabble 65 has a built in 62 key typewriter-style keyboard. The keyboard is read by polling the rows and columns that the keys are





RESET ROUTINES	PB6	PB5	PB4
NORMAL 64×32	Ø	Ø	Ø
NORMAL 80×25	Ø	Ø	1
ROM BASIC	Ø	1	Ø
ROM FORTH	Ø	1	1
DISK BOOT 64×32	1	Ø	Ø
DISK BOOT 80×25	1	Ø	1
SERIAL TERMINAL	1	1	Ø
USER RESET	1	1	1

VECTOR TO $EØØØ

*OPTIONAL TRACE-ON/OFF SWITCH IN LATER RELEASES

RABBLE 021 COMPUTERS	
RABBLE 65	
KEYBOARD	
CHECKED RG	DRAWN K.A.G.M.
APPRVD BY W.J.C.	AUGUST 1983

connected to. This method of reading the keyboard is extremly economical as the 62 keys can be individually read with only 20 wires arranged to connect the keys in a 12 x 8 matrix.

The matrix is connected to the ports of a 6532, RIOT, and 6522, VIA, where the software / monitor reads which column and which row have been connected together. Once a key has been read into the RIOT and VIA, the monitor converts this value to ASCII value for use by the computer. The RIOT for the keyboard is located at $C4XX which is decimal 50176, The VIA for the keyboard is located at CO6X which is decimal 49608

Some of the keys on the keyboard do not generate on ASCII code, but instead are used to extend the range of control of the keyboard.

CONTROL and SHIFT are used to modify the codes produced by the other keys. The chart, below, shows the codes produced when SHIFT or CONTROL are pressed with another key.

The RIOT contains 128 bytes of RAM as well as the input output ports as found on the 6521 and 6522, a timer is also included within this chip although it is not utilised in our application.

The RAM is used as a line buffer for keyboard entry, and this is located from $C400 - $C47F

Sixteen function keys are provided for. These keys are along the top of the standard keyboard, and labelled F1 through to F16. They provide the ability to customise software for ease of operation, whilst permitting great flexibility in the control of the system.

The function keys have been extended to provide external control of the keys F1 - F5 and F9 - F13. The connectors for these keys are suitable for joystick controls, making games software much more realistic in operation. CHAPTER 6

VIDEO DISPLAY CONTROLLER

ASSEMBLY

The video display controller is the most complex section of the Rabble 65. There are 17 chips used in this section of the computer, and to facilitate the assembly and gain an understanding of the operation, the circuits have been split into two areas. These are the parallel and serial sections.

The parallel side of the video display controller deals with the data from the CPU buss and the CRTC in the parallel mode, prior to conversion to serial format. This includes the converting of ASCII data to the video character data. The serial section contains the parallel to serial shift register delay lines, buffering, and vertical and horizontal sync. mixing.

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To assemble, the following sockets must be fitted:-

Parallel stage	IC's	53 - 58 Inclusive
	IC's	70 - 73 Inclusive
Serial stage	IC's	69 and 81 - 86 inclusive

Note the orientation of all sockets. To avoid later confusion, pin No. 1 of each socket is located towards the back edge of the board. The IC type No. is printed at the pin one end of the chip. Install the 3 resistors and the video connector.

After all components are soldered in place, inspect that no solder splashes, blobs etc. exist. Clean down any resin deposits by carefully wiping with a cloth dampened with methylated spirits.

Insert each chip into its appropriate socket to complete assembly. There are no hardware adjustments to be made to the video display controller as the CRTC is a software controlled device.

VIDEO DISPLAY

DISPLAY TYPE	:	MEMORY MAPPED SYSTEM RAM $D000 - $D7FF
DISPLAY CAPACITY	:	2048 Characters
CHARACTER SET	:	UPPER and LOWER CASE ASCII and GRAPHICS
CHARACTER TYPE	:	8 x 8 DOT MATRIX
VIDEO OUTPUT	:	1v P-P COMPOSITE VIDEO
DISPLAY FORMAT	:	64 CHARACTERS x 32 ROWS 80 CHARACTERS x 25 ROWS (Software selectable)

Connection of the Rabble 65 to the video display monitor is via an RCA phono jack on the rear of the computer case. Your connector cable will be required to mate with the RCA phono jack to be compatible with your monitor at the other end.

It is recommended, for best results, to use a high quality video monitor rather than a converted TV set for your video display. The dot rate of our video generator is running at 16 Mhz, whereas few TV sets are designed to run at more than 4 Mhz. This does not mean that a TV set will not operate, however, the definition of the data on screen will be poor. For the same reason we do not recommend the use of VHF/UHF modulators

SCREEN FORMAT

The screen format is set up for 32 rows of 64 characters per row. This is the standard format for all standard application programmes. Another format is provided for in the system ROM, it is 80 x 25 for those wishing to operate their Rabble 65 as a terminal. To select the 80 x 25 screen format, the system monitor reads the system VIA Port B, bits 4 - 6. The system is initialised according to the code on these lines. For further information on the initialisation options, refer to the chapter on the keyboard.

SCREEN MEMORY

The video display requires 2048 bytes of RAM, IC 72, located at $D000 - $D7FF. The video display uses this RAM to store information required to be printed on the screen. The CRTC, IC 57, cathode ray tube controller, takes the information from the memory and sends it to the character generator which converts the ASCII data to a format suitable for conversion to serial format to provide the dot information on the screen. A dot is sometimes referred to as a pixel or picture element.

The character generator provided with the Rabble 65 is a 2732 ROM. This ROM has 512 individual characters stored for use by the user. The ASCII character set in upper case, lower case and many control and function signs are implemented, together with numerous graphics symbols to provide adequate animation facilities for the user. The video character generator is used to store two sets of characters, of which only one set is available at a time. The selection of the alternate character set is controlled by bit 2 at port A on the system VIA located at $C06X. A high on this bit selects the alternate character set. The standard character set, which is initialised on reset is selected with a low bit on Port A, bit 2 of the VIA.

CIRCUIT DESCRIPTION

The CRTC based video is capable of receiving a digital input, processing it, and displaying the appropriate alpha numeric or graphic data on a video monitor. The timing for the system is derived from a dot clock oscillator. The frequency of the dot clock is 16 Mhz, and this is used to drive the whole Rabble 65. The dot clock is fed to the 74LS166, IC69, parallel to serial shift register to control the rate of flow of information to the screen. The dot clock oscillator is divided down to generate the character clock. Thus for an 8 x 12 dot character display format the dot clock is divided by 8 to produce the character rate clock. The divider used for this purpose is a 74LS163, IC58, synchronous 4 bit counter. The 4 Mhz output of the counter is fed to the 6845, IC57, and is used for the CRTC clock where all the timing within the video system is referred. Each character rate clock increments the address lines (MA0 - MA10) of the 6845. The 6845 has 13 address lines, our application uses 10 of these.

The video display RAM must be able to be accessed by both the CRTC

and CPU. Therefore, the address lines are multiplexed between the two devices via the 74LS157's,IC's 54, 55 and 56. The CPU takes control of the memory only during periods of reading from or writing to the video memory. The output of the multiplexer drives the RAM address lines.

The 2K x 8 static display memory is a CMOS 6116LP3 RAM chip as used throughout the Rabble 65. This memory requires lines which select a particular memory location within the RAM. The output of the display RAM (the data buss) is fed to an 8 bit latch (74LS374), IC 71, and is clocked into the latch on the next character clock. The character clock is used to latch the data into the 74LS374, IC 71. This creates a delay of one character clock from the time an address becomes valid to the memory, until the data is presented to the character generator ROM. The character clock also loads the parallel data from the character generator ROM into the shift register. This produces a second character clock delay. Once the shift register is loaded (74LS166) IC 69, the dot clock is used to shift data from the shift register to the video driver in serial format.

The display enable, DE and cursor, CURS, output signals are synchronous with the CRTC address lines. These signals are delayed by two character clock pulses to produce the signals on the video screen at the correct spots. To produce the required delay the signals DE and CURS, are fed via two flip flops (74LS175) IC 86, each clocked by the character clock, and the outputs are then fed into the video driver. The video signal is the combination of the shifted data ORed, IC 84, with the cursor and then ANDed, IC 83, with the display enable. This is fed into a 74LS74, IC 82, "D" flip flop and the signal is clocked out by the dot clock, to the open collector inverter, IC 81, this signal is then mixed with the H sync, and V sync, to provide a composite video signal suitable to drive a video monitor.

The CRTC generates character row addresses (RA0 - RA4) for the character generator ROM. Selection of these addresses is synchronised within the CRTC by the horizontal sync pulse (H sync). The row address is incremented by one each H sync.

When the CPU is required to read from or write to the display RAM. the address multiplexer is switched to the CPU address lines. Since the display memory is located from $D000 to $D7FF, the chip select line (CS) labelled D000 is used to connect the address buss and the data buss to the CPU's busses. The address buss is connected to the video RAM via three 74LS157's, IC's 54, 55 and 56, two to one demultiplexers, the data buss is connected via a tri-state bidirectional buffer 74LS245, IC 73. With the data and address buss connected to the CPU, the video RAM is under the control of the CPU and the contents of the video RAM is treated as ordinary read-write memory. However, it is usual to store only information for display on the VDU in this RAM.

The 6845 CRTC, IC 57, used on the Rabble 65 is a software controlled device and can thus be programmed for screen formats other than the 64 x 32 and 80 x 25 which we have provided. Further formats and function changes can be invoked by the user. The CRTC has an address register that can point to any one of eighteen buried registers within the CRTC. Some of the variations which can be invoked by altering the registers which are addressed within the block $C01C - $C01F, decimal 49180 - 49183, are

a screen format of 256 characters per row and 128 rows per screen. The horizontal and vertical sync positions are programmable, this allows the movement of the standard screen format to centre it on your monitor if necessary. Size and format of the displayed character block can be altered to provide a myriad of formats. The cursor can even be programmed to blink.

The registers in the CRTC are labelled R0 - R17, the following list briefly describes the function of each, and the value it contains for the Rabble 65 32 x 64 screen format.

R0 - HORIZONTAL TOTAL REGISTER which contains the sweep plus retrace time of one horizontal line

R1 - HORIZONTAL DISPLAY REGISTER - contains the number of characters to be displayed per row and should not exceed 80% of the value in R0.

R2 - HORIZONTAL SYNC POSITION REGISTER is programmed in character times and should be positioned such that it will occur slightly after the CRT beam is driven past the right edge of the screen.

R3 - HORIZONTAL SYNC WIDTH REGISTER also in character times, should be longer than sync circuitry in your monitor. It is normal for the value in R0 to be greater than the sum of R2 and R3.

R4 - VERTICAL TOTAL REGISTER contains the number of character rows per screen, which is equal to the number of scan lines divided by the height of the character block.

R5 - VERTICAL ADJUST REGISTER holds the number of scan lines not required for display purposes.

R6 - VERTICAL DISPLAYED REGISTER has stored in it the number of character rows that are required for display.

R7 - VERTICAL SYNC POSITION REGISTER is programmed in

...

character times and sets the position of the vertical sync pulse. The value must be equal to or greater than that of R6, but not too much greater than R6, lest the bottom rows will disappear.

R8 - INTERFACE MODE REGISTER set the screen for normal sync, interlace sync or interlace sync and video. Normal sync writes to the screen with repetitive vertical sweeps which are not interlaced. Interlaced sync produces a similar display to the previous method but with interlaced raster scans. The last method, interlaced sync and video produces half height characters.

R9 - MAX SCAN LINE REGISTER holds the total number of scan lines per field.

R10 - CURSOR START REGISTER set the scan line on which the cursor will begin. One bit of this register specifies wether the cursor will blink or not, and another bit sets the blink rate at 320 ms or 640 ms.

R11 - CURSOR END REGISTER holds the scan line on which the cursor will end. If the same as R10, then the cursor is only one line tall.

R12 - R13 : START ADDRESS REGISTERS HIGH and LOW contains the address of the first byte of RAM to be displayed after vertical retrace.

R14 - R15 : CURSOR REGISTERS HIGH and LOW contain the address of the cursor position in video memory.

R16 - R17 : LIGHT PEN REGISTERS HIGH and LOW hold the address appearing on the CRTC address lines when the light pen strobe input pulses high. The light pen has not been implemented on the Rabble 65.

NOTE: The character clock rate will be the product of the horizontal oscillator frequency and the total horizontal

..

character times described in calculating the value for R0. The dot clock will be the product of the character rate clock and the width of the character block in columns. This may dictate a different dot clock for other screen formats.

DEBUGGING

If any malfunction is suspected in the operation of the video display controller, you should confirm that the following sections are operating correctly, for a malfunction in any of these areas can inhibit the normal operation of the CRTC. the areas to check are:-

CPU
RAM 1
Monitor ROM.

Refer to these sections if you are unsure of their operation.

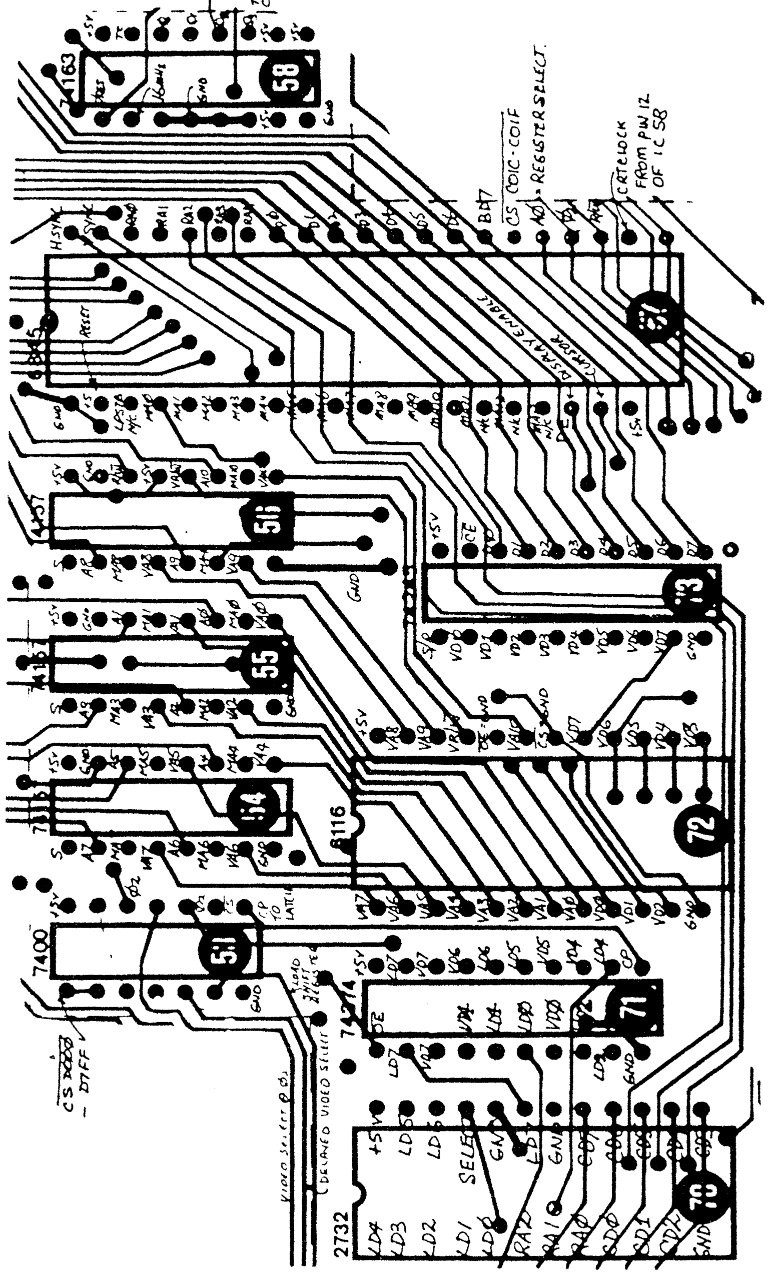
Address lines from the CPU buss must reach both the video RAM and the CRTC. This is controlled by IC's 54, 55 and 57, 74LS157 data selectors. Check that the select input of each of these chips, pin 1, goes low when CS$D000 is accessed, decimal 53248. When the select pin is low the address lines from the video RAM are connected to the CPU buss, and when this select line goes high the video RAM address lines are connected to the CRTC, 6845 IC57.

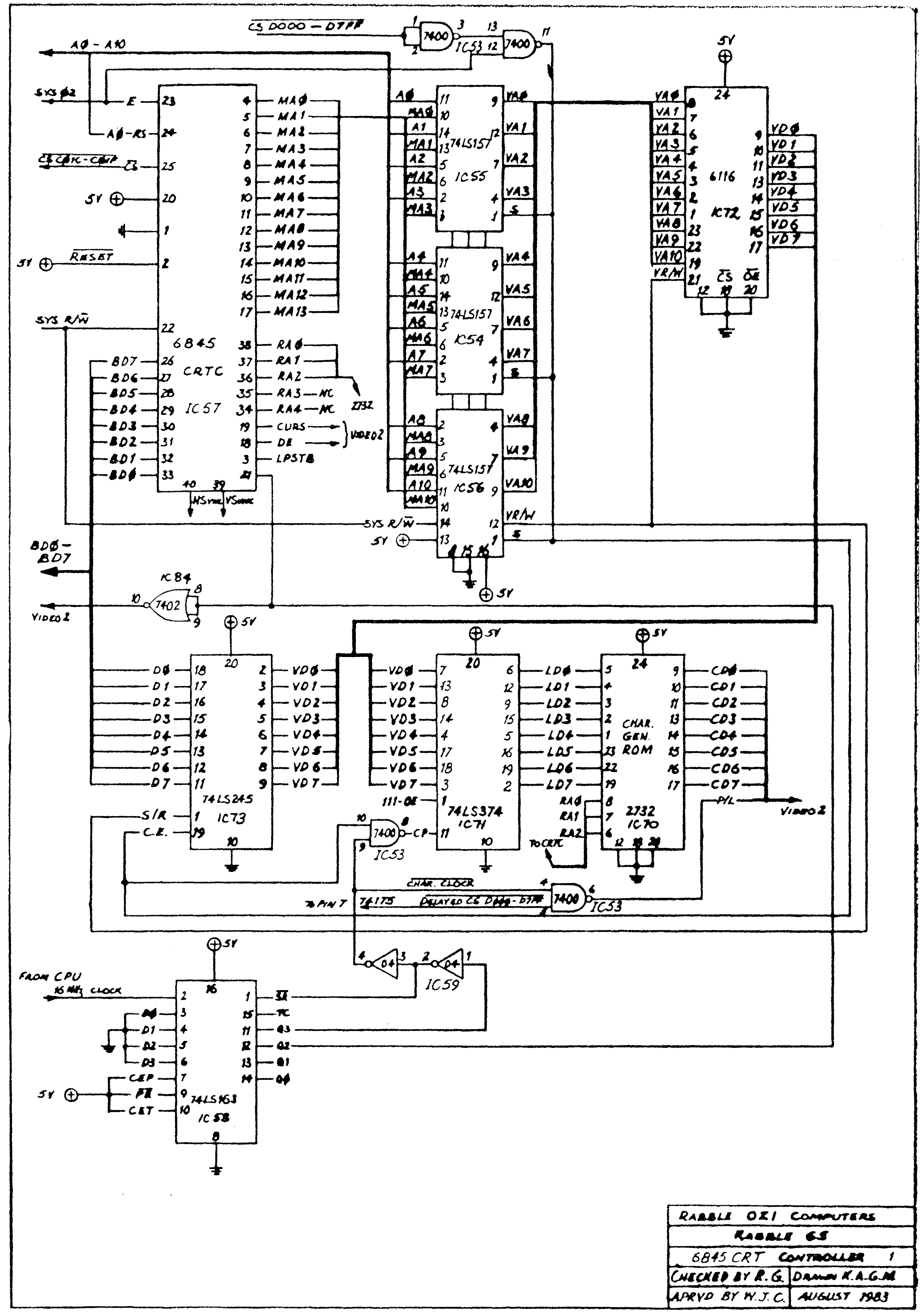
Data line transceiver IC73, 74LS245 is also controlled by the CS$D000 line to connect the data buss to the CPU. Pin 19 of IC73, when low, enables the transceivers to permit data to flow in one direction or the other depending on the status of the R/w line. This enables data transfer between the video RAM and the CPU buss.

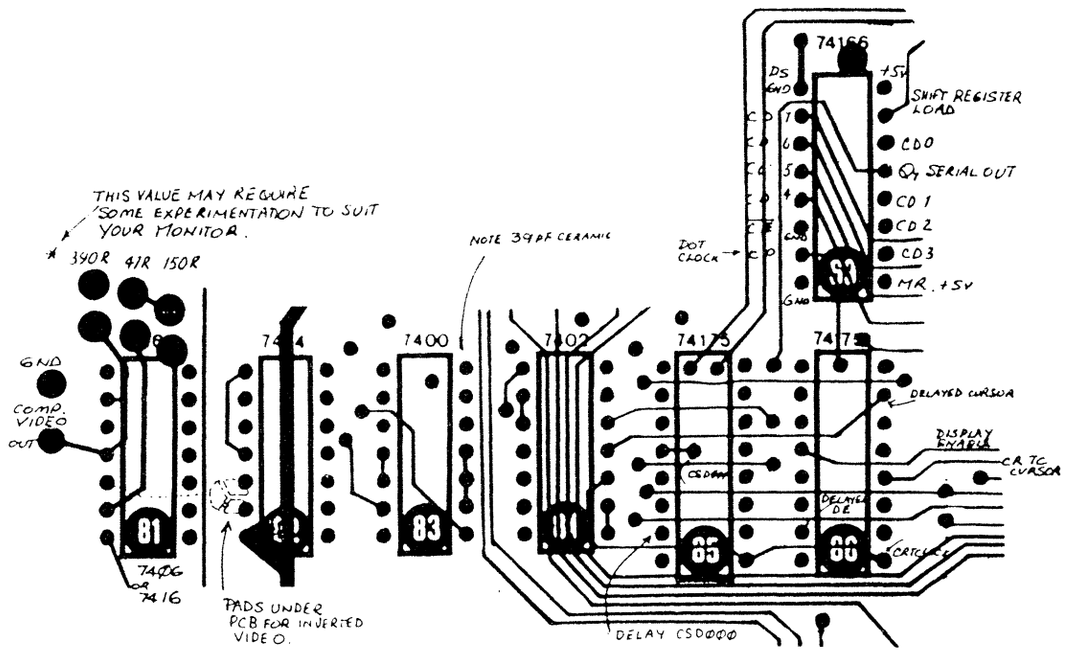
Ensure that the CS$C01C, decimal 49180, is reaching pin 25 of the CRTC, 6845 IC57. Test pin 24 for system address line A0, test pin 23 for phase 2 clock and pin 22 for the R/w signal. If all these signals are normal, and the reset line, pin 2 goes high for the duration the reset key is pressed, read the registers in the CRTC to ensure the expected values are contained therein. If the expected data is not in the registers, it is most likely that your screen is not displaying a readable format. in this case check that the following signals are present at the indicated test point.

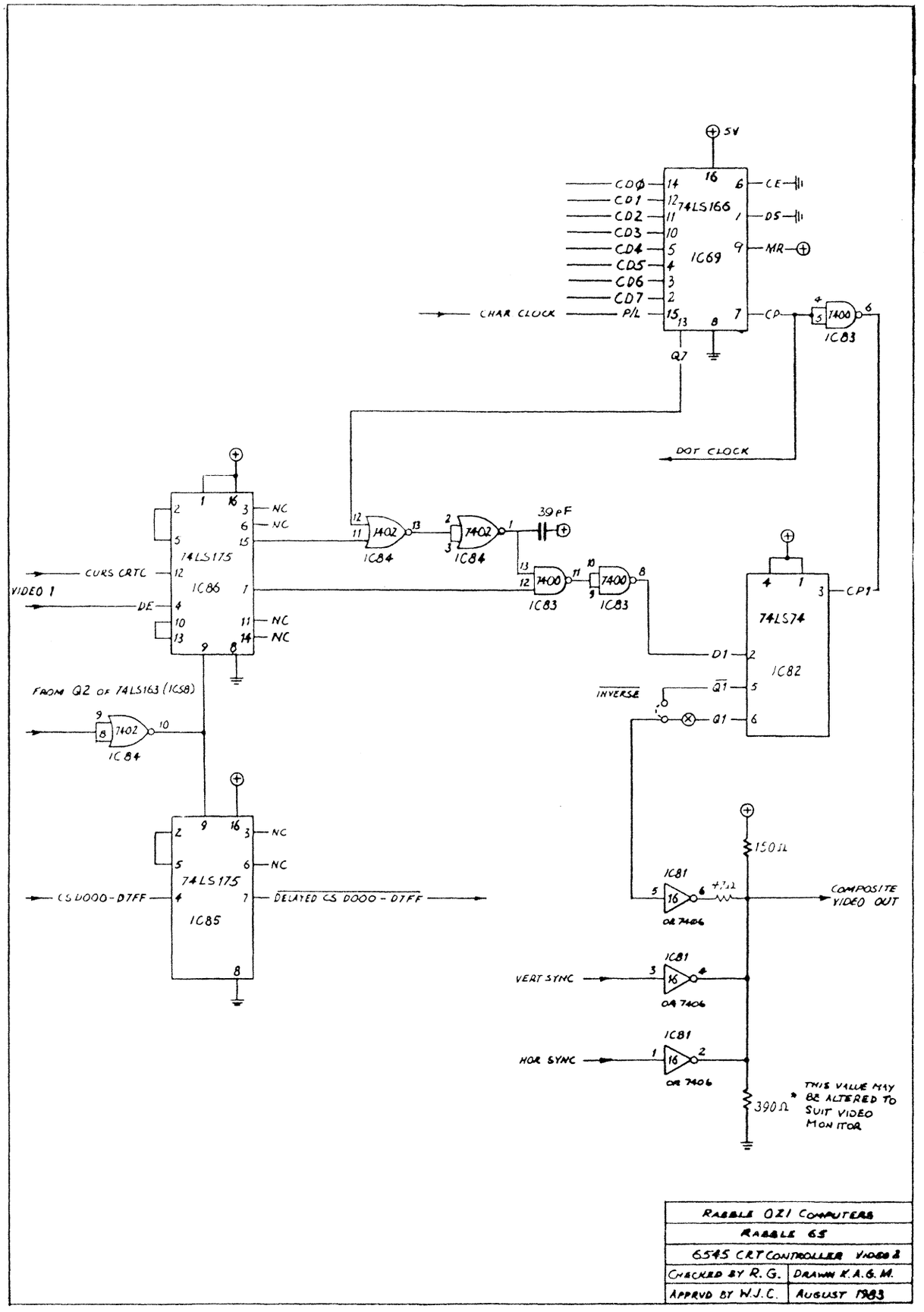
	Test point			Expected signal
1	pin 3	IC 82	74LS74	16MHz clock
2	pin 7	IC 69	74LS166	16MHz clock
3	pin 13	IC 69	74LS166	16MHz serial data
4	pin 15	IC 69	74LS166	character clock
5	pin 11	IC 71	74LS374	character clock
6	pin 7	IC 86	74LS175	cursor
7	pin 15	IC 86	74LS175	display enable
8	pin 1	IC 81	7416	H.Sync.
9	pin 3	IC 81	7416	V.Sync.
10	Video connector			Composite Video.

In any of the above test points, should a signal be missing, check the previous stage, then work back through the circuitry to determine the faulty chip. Replace any suspect or faulty chips as required.




RABBLE OZI COMPUTERS
RABBLE 65
6845 CRT CONTROLLER 1
CHECKED BY R.G.
DRAWN K.A.G.M.
APRVD BY W.J.C.
AUGUST 1983


THIS VALUE MAY REQUIRE SOME EXPERIMENTATION TO SUIT YOUR MONITOR.
* 390R 4/R 150R
GND
COMP. VIDEO OUT
74LS04
7400
7402
74175
74166
NOTE 39pF CERAMIC
DOT CLOCK
DS
GND
+5V
SHIFT REGISTER LOAD
CD0
SERIAL OUT
CD1
CD2
CD3
MR. +5V
DELAYED CURSOR
DISPLAY ENABLE
CR.TC CURSOR
CRTC CLK
DELAY CSDDDD
74LS06 OR 7416
PADS UNDER PCB FOR INVERTED VIDEO.


+5V
74LS166
IC69
CD0
CD1
CD2
CD3
CD4
CD5
CD6
CD7
P/L
CHAR CLOCK
CE
DS
MR
CP
Q7
7400
IC83
DOT CLOCK
74LS175
IC86
CURS CRTC
VIDEO 1
DE
NC
7402
IC84
39pF
74LS74
IC82
CP1
D1
INVERSE
Q1
FROM Q2 OF 74LS163 (IC58)
CS DOOO-D7FF
DELAYED CS DOOO-D7FF
IC85
150Ω
IC81
74LS06 OR 7406
COMPOSITE VIDEO OUT
VERT SYNC
HOR SYNC
390Ω
* THIS VALUE MAY BE ALTERED TO SUIT VIDEO MONITOR
RABBLE 021 COMPUTERS
RABBLE 65
6545 CRT CONTROLLER VIDEO 2
CHECKED BY R.G.
DRAWN K.A.G.M.
APPRVD BY W.J.C.
AUGUST 1983

CHAPTER 7

SERIAL INTERFACE

ASSEMBLY

The serial interface can be constructed as an RS232 interface, cassette interface or both. IC's 96, 97, 112, 113, and 114 are common to both modes. IC's 93 and 94 are used only in the RS232 mode and IC's 64, 65, 95, 110 and 111 are used only in the cassette mode.

To assemble this stage, all IC sockets should be mounted, then all discrete components required for the options selected. There are two resistors for the RS232 mode and five resistors, six capacitors, two diodes and a trimpot for the cassette mode. Once all relevant sockets and components are mounted, check all soldering for cleanliness before proceeding.

Insert IC's 90, 97, 112, 113 and 114. These chips are common to both modes. Test IC's 90, 97, 112 and 113 by checking that a waveform appears at pins 3 and 4 of the ACIA, IC 114. Test CS F000 / FC00 line on pin 9 of the ACIA by accessing $F000 or $FC00 , decimal 61440 or 64512, to ensure that the chip will be selected.

Fit the relevant IC's for the RS232 and / or cassette interface as required. The RS232 requires no further adjustments. The cassette interface requires no adjustment for transmit and only one minor adjustment for receive. The adjustment detailed is to provide a receive signal conversion for 300 Baud data.

1. Connect 1200Hz from pin 3 of IC 112, 74LS393, to pin 20 of the Molex interface connector.

2. Connect a CRO to pin 13 of IC 95, 74LS123.

3. Adjust trimpot adjacent to IC 95 to obtain a 600uS positive going pulse on the CRO.

An alternative method of setting this input to an approximate setting if a CRO is not available, is as follows.

1. Connect a cassette recorder to the input of the serial port.

2. Load the prerecorded cassette programme, by pressing RESET then select ROM BASIC by pressing the space bar and then R. Type LOAD then press the return key.

3. Start the cassette recorder, and adjust the trimpot slowly

until the text appearing on the screen becomes readable. Rotate the trimpot until it starts to garble the data and then find the central point between the two extremes of "good" data. this completes the adjustment.

CIRCUIT DESCRIPTION

The RS232 / cassette interface is located at both $F000 - F001 and $FC00 - FC01. The RS232 I/O is via a 25 way standard connector, the DB25PSAA. The relevant connections are wired to the international standard.

The RS232 I/O has a software selectable Baud rate derived from the system 16MHz clock. This clock is divided down to 4MHz in the video block and fed to the Baud rate divider. The 74LS393, IC 112, and IC 113, 74LS00, divides the 4MHz clock by 13 to provide a 125nS pulse to the 4040, IC 96, every 3.25uS. The 4040 divides this by factors of 2 through to 256 to provide eight Baud rates from 75 to 9600 Baud.

Between the 4040, IC 96, and the ACIA, IC 114, is a demultiplexer, IC 97 a 4051. This device connects only one of the eight Baud rate outputs of the 4040 to the clock inputs of the ACIA. The selection is performed by setting up the system VIA port A bits 5 - 7 with the required data.

Baud rate	VIA PA Bit 7 6 5
75	0 0 0
150	0 0 1
300	0 1 0
600	0 1 1
1200	1 0 0
2400	1 0 1
4800	1 1 0
9600	1 1 1

The system VIA is located at $C060 and is initialised on the standard system for 300 Baud. This also sets the cassette interface to 300 Baud.

The ACIA, IC 114 receives data from the data buss and converts this to the serial form and transmits it via the Tx data output to an RS232 line driver, MC1488 - IC 93. This line driver converts the TTL signal to true RS232 standard, which has a voltage swing of +12 volts to -9 volts, compared with a TTL voltage swing of +3.5 volts to +0.6 volts approximately This occurs when the R/w line is low. When the R/w line is high, data is read from the RS232 connector via the MC1489, IC 94, RS232 to TTL convertor, and the fed to the ACIA Rx input. The data on this input is clocked into the receive data register and when it is full a signal is generated within the the ACIA to indicate this status to the CPU. The ACIA loads this, now parallel, data onto the data buss at the request of the CPU, ie a read from the ACIA.

...

Three control signals are used with the ACIA for the RS232, the Data Carrier Detect (DCD), Clear To Send (CTS) are input signals and the Request To Send (RTS) is on output.

The DCD input is active low and it inhibits and initialises the receiver section of the ACIA when high. A low to high transition of the DCD initiates an interupt to the CPU to indicate the occurence of a loss of carrier when the Receiver Interupt Enable (RIE) is set.

The CTS input provides automatic control to the transmitting end of a communications link via the CTS, active low, by inhibiting the Transmitter Data Register Empty (TDRE) status bit.

The RTS output enables the CPU to control a peripheral, via the data buss. The RTS is active low and is controlled by the contents of the ACIA control register.

Other signals as shown on the circuit of the RS232 connector are not used on this system.

The cassette interface is designed to operate at 300 Baud and is initialised on system RESET to operate at this speed. 4800Hz is fed into IC 112, 74LS393, and this is divided down to provide 2400Hz and 1200Hz signals. The 2400Hz clock and the Tx data from the ACIA, IC 114 are fed to a 74LS74,D type flip flop and data inputs respectively. Each 833uS the information on the data input is clocked out of the flip flop and the Q output is set if the data is logic one and if the data is logic zero, the Q output is reset to logic o. If the Q output is set, the 2400Hz AND gate is enabled and thus eight cycles of the 2400Hz signal are output to the cassette via pin 3 of the Molex connector. If a logic zero is input to the flip flop the Q output is reset and the 1200Hz gate is enabled, causing four cycles of 1200Hz to be output to the cassette.

To read data from cassette the information is fed via pin 5 of the Molex connector. This signal is clipped to 0.6 volts P-P by the IN914 diodes prior to amplification by the CA3130, IC 64, amplifier. The signal is then buffered by a pair of 74LS00 gates, IC 65, prior to being fed to the retriggerable monostable multivibrator IC 95, 74LS123, and the clock input of flip flop IC 110, 74LS74. These clock signals are 2400Hz, to represent a logic one data bit or 1200Hz for a logic zero data bit. With each positive going pulse into the 74LS123, IC 95, a fixed length pulse is fed to the clear data input of the flip flop, IC 110, as well as its data input. This data is transferred to the Q output of the flip flop on the next clock pulse input to the clock input of the flip flop. For a 2400Hz signal the 74LS123 monostable is retriggered prior to it completing its output pulse. The duration of the monostable pulse is approximately 600uS. For 2400Hz signal input the 74LS123 is reset each 417uS, thus causing the output to remain at logic one. A 1200Hz signal, which represents logic zero, has a period of 833uS. Thus for a 1200Hz input signal, the Q1 output of IC 95, 74LS123, goes high for 600uS and the Q output of IC 110, 74LS74, has the previous signal data transferred to it. At the next positive going edge of the 1200Hz signal the monostable is reset and the logic zero signal at the data input, pin 12 of IC 110, is transferred to the Q output and carried to the ACIA, IC 114, serial input, pin 2.

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DEBUGGING

The programmable divider is a chain of dividers followed by a one-of-eight selector. IC 112, 74LS393, should have a 4MHz square wave input to pin 13, and a pulse output of approximately 125nS width each 3.25uS. This pulse should be present on pin 10 of IC 96, 4040. The outputs of the 4040 should exhibit a frequency of 16 times the Baud rate shown on that output. The demultiplexer, IC 97 4051, will have an output frequency of 16 times the actual selected Baud rate. The selected Baud rate is determined by IC 107, VIA, and the table of values is shown in the circuit description of this chapter. This area must function correctly before the rest of the serial interface can be expected to perform.

The ACIA, IC 114, has eight data lines which should have data signals to it when written to. Control signals should be present, these are phase 2 clock, pin 2; R/w, pin 13; address line A0, pin 11; and CS on pin 9. The CS line can be accessed by addresses $F000 or $FC00, decimal 61440 or 64512.

Write to the ACIA after a standard system initialisation and ensure that data is output in serial format on pin 6 of IC 114, ACIA. This data should also be found on pin 2 of the DB25PSAA connector.

Connect pins 2 and 3 of the DB25PSAA connector together and then write to the ACIA again and the serial data should appear on pin 2 of the ACIA, IC 114.

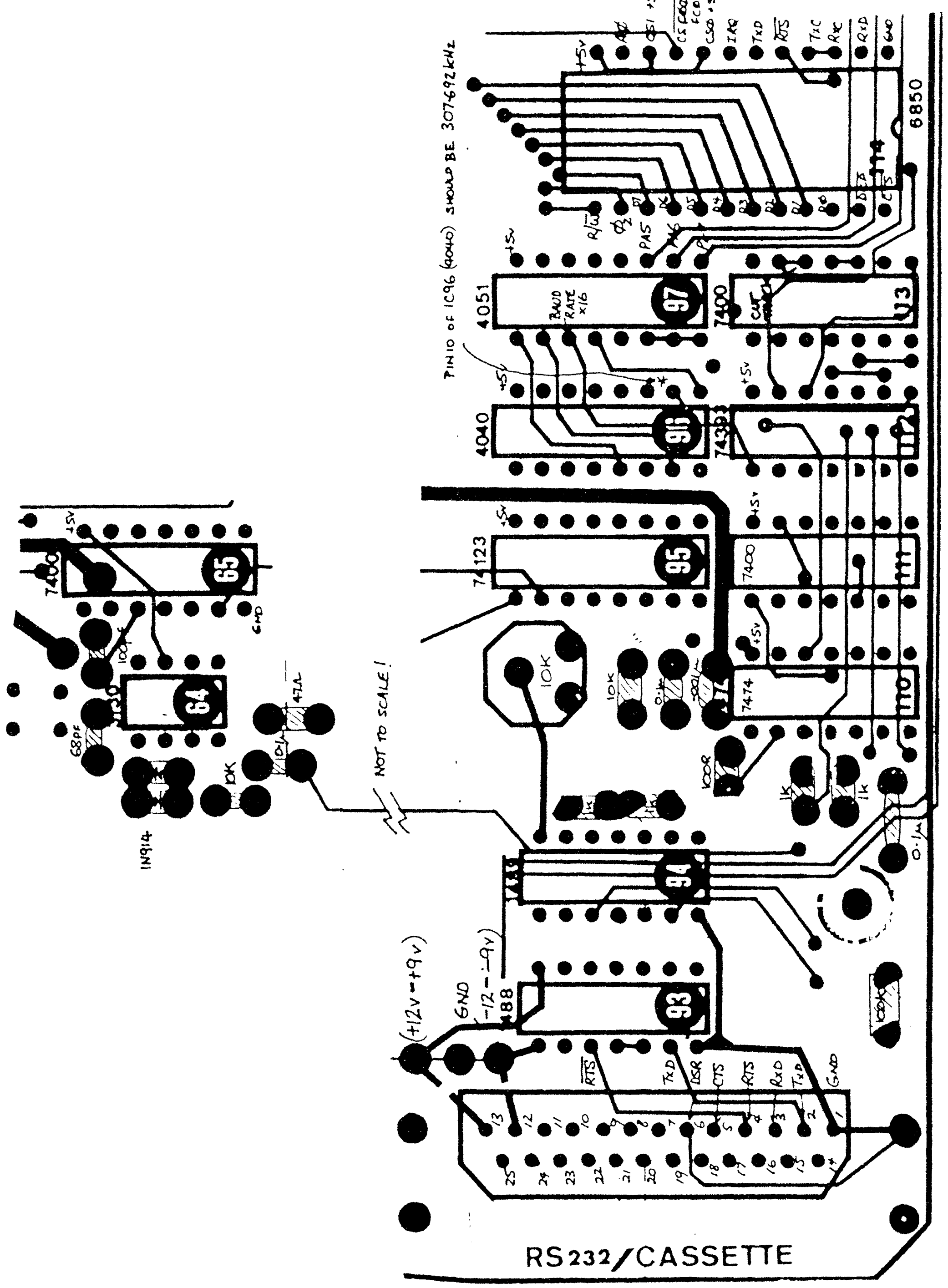
Pins 5 and 8 of the DB25PSAA connector should be floating high and the inputs of the ACIA, pins 24 and 23 of IC 114, should be low. These are the inverting, level translator gates of IC 94, MC1489.

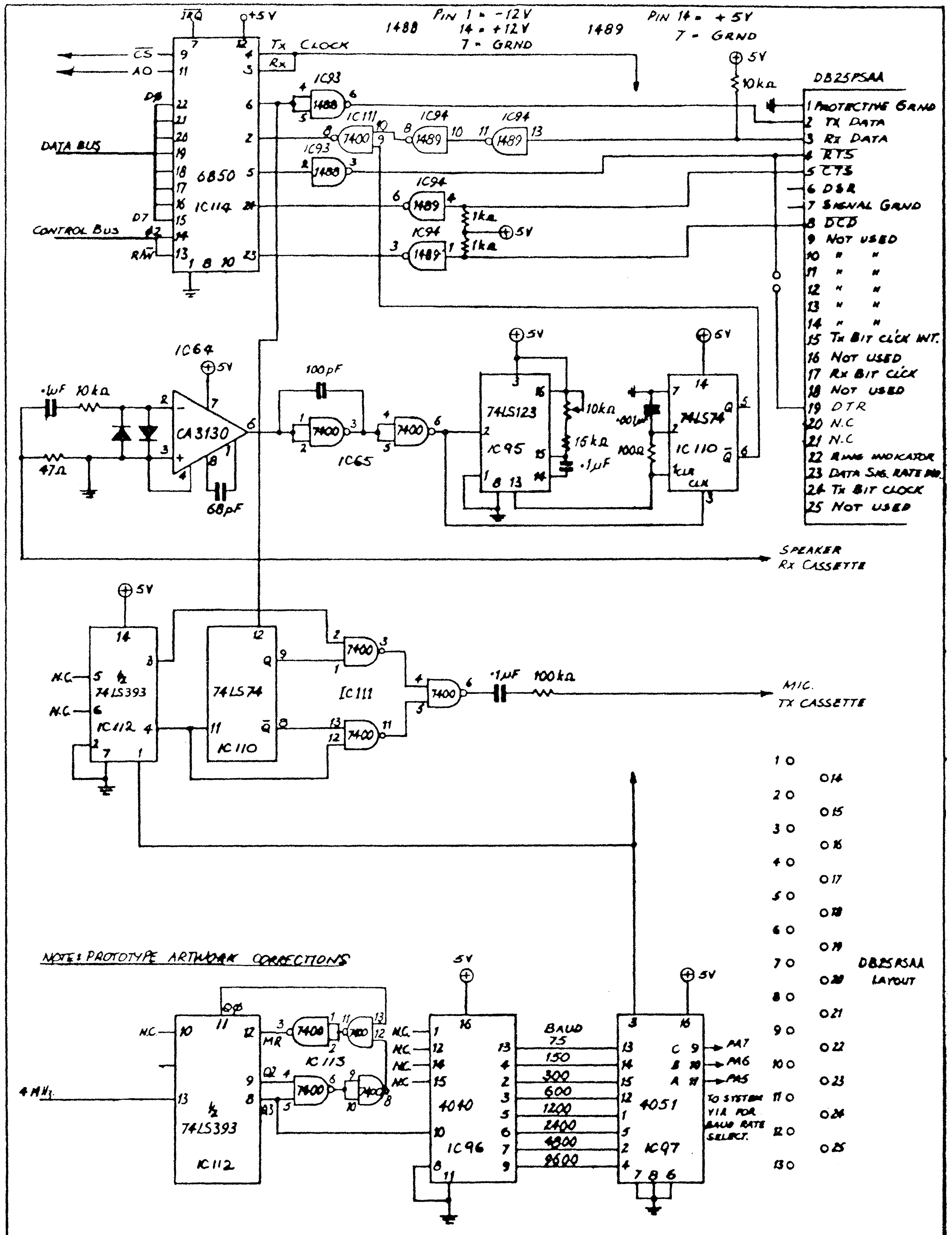
After ensuring that the RS232 section works, ensure that the 1200Hz and 2400Hz signals are present on IC 112, 74LS393, pins 4 and 3 respectively. Serial data at 300 Baud should be present on pin 12 of IC 110, 74LS74 and the outputs on pins 9 and 10 should toggle with data changes. Pin 9 of IC 110 should be logic one when a data bit is logic one and pin 10 should be logic zero when a data bit is logic zero. Follow this data stream through the 74LS00 gates, IC 111, and finally to appear on pin 5 of the Molex connector.

To test the cassette receiver connect pins 3 and 5 of the Molex connector together and output data to the port. Check that the signal reaches pin 2 of the CA3130, IC 64, and that it does not exceed 0.7 volts P-P. The input waveform from cassette recorders may be somewhat distorted, but should square up once they pass through this amplifier. Pin 6 of IC 64 should exhibit a square waveform alternating between 1200Hz and 2400Hz. This same signal should appear on pin 2 of IC 95, 74LS123 monostable multivibrator, and also on pin 3 of IC 110, 74LS74 flip flop.

If all is well at this point, ensure that the set up instructions detailed in the assembly instructions have been carried out, or if unsure, carry out the set up again.

Data into pin 13 of IC 110, 74LS74, should be data in serial format at the rate of 300 Baud. This data stream is also expected at pin 6 of IC 110, prior to ORing with the RS232 signal, from the gates of IC 94. This signal is then fed to the ACIA at pin 2.





(C) PA7	0	0	0	0	1	1	1	1
(B) PA6	0	0	1	1	0	0	1	1
(A) PA5	0	1	0	1	0	1	0	1
	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
BAUD RATE	75	150	300	600	1200	2400	4800	9600

RABBLE OZI COMPUTERS	
RABBLE 65	
SERIAL INTERFACE	
CHECKED BY R.G.	DRAWN K.A.G.M.
APRVD W.J.C.	AUGUST 1983

CHAPTER 8

CENTRONICS PARALLEL PORT

ASSEMBLY

This section of the Rabble 65 computer is straight-forward, as there are no timing adjustments to be performed. The interface consists of only four chips, a connector, three resistors one resistor pack and a capacitor. To assemble this section, ensure that the Centronics port connector and the IC sockets, No's 63, 78, 79 and 80, are installed. Fit into position the discrete components and the resistor package, taking care to orientate the resistor package the correct way around. Pin 1 of the resistor package will be identified by an indentation on the package at the pin one end or with a spot at the same end, this end is fitted to the rear of the board, away from the keyboard. Check all solder connections to ensure no tracks are shorted or pins are left unsoldered. If neccessary clean excess resin from the board with a cloth dampened with methylated spirits. When satisfied all is well insert IC's 63 - 74LS123, 78 and 79 - 7417, and 80 - 6821.

CIRCUIT DESCRIPTION

The heart of the Centronics interface is the 6821, IC 80, which is a PIA. This chip is located at memory address locations $F400 - F403, decimal 62464 - 62467, and contains registers which are initialised by the system after resetting. Address lines A0 and A1 are used to select the appropriate register when the CSF40x line is held low. The R/w line is used to store data from the data buss into the registers during a write cycle or to read data during a read cycle. The reading or writing to the output registers of the PIA causes the transfer of data to or from the Centronics port. Port A output register is located at $F400 and port B at $F402.

The PIA in this application is organised to set up Port A bits 0 - 5 as inputs, and bit 7 as an output. Port B is organised to set all bits as outputs. Port A bit 6 is unused.

CA1, CA2, CB1 and CB2 are not extended to the Centronics port, and thus an interupt request (IRQ) cannot be generated.

The PIA is automatically reset on system power up, and is initialised by the system monitor.

All data and control signals output by the Centronics interface are buffered IC's 78 and 79, 7417 - open collector buffers, with pull up resistors on their outputs. This provides around 20mA of sinking capability, which will suit a wide range of parallel printers.

The 74LS123, IC 63, retriggerable monostable multivibrator is used to provide a STROBE signal to advise the printer that valid data is on

the Centronics data buss, at that point of time. The STROBE signal is initiated by a CPU access to address $F420, decimal 62496. This causes the input line CSF42x to IC 63 to go low and enables the monostable to generate a pulse of around 1uS, determined by the values of the R and C of the monostable. In our application the resistor is 15Kohms and the capacitor is 220pF. The STROBE signal is a negative going pulse from the output of IC 63, and is bufferred by the 7417 buffer prior to being output on the Centronics connector.

To output data to the printer the system software reads the data on Port A and tests that the printer is ready to receive a character or byte of information, and, if ready, a data byte is loaded into Port B output register of the PIA, IC 80. This then appears on the Centronics interface connector. A print STROBE pulse is then generated as described earlier, advising the printer to read the data from the data buss. The printer then generates a printer BUSY signal to prevent the Rabble 65 from outputting any more characters. This condition is held until the printer has completed printing the character or has stored it in its own memory buffer. During the BUSY signal condition, the CPU continually tests and waits for the BUSY signal to be cleared before setting the PIA up for the next character to be printed.

Other signals are available on the Centronics printer to indicate the status of the printer, and can be tested the system software as required. These are FAULT, SELECT, PAPER OUT and ACKNOWLEDGE.

DEBUGGING

Ensure that the STROBE signal is present by writing to $F420 and monitoring pin 1 of the Centronics connector with a CRO or logic probe. A negative going pulse of greater than 0.5uS should be visible each time $F420 is accessed. If this is missing check for it at the output of IC 63, pin 4, and if still missing check that the CSF420 signal is reaching pin 1 of IC 63, to enable the monostable. Replace IC 63, 79 or associated components as required, to restore the STROBE pulse.

Assuming the STROBE pulse is normal, check that there are no irregularities in the printers operation, ensure that it is turned on and selected for the correct format etc. If it has a self test function then ensure it passes that test. Next check with a CRO or logic probe that the BUSY line is low, if not the CPU will wait for the printer to send it high before attempting to output a character.

If all PIA input signals test correctly, initialise the PIA by resetting the CPU with the standard Rabble 65 monitor, the RA65. Examine the relevant memory locations to ensure that the PIA is functioning correctly.

Address	Data	
F400	00	with printer disconnected
F401	04	
F402	xx	depends on data being

...

29....
output

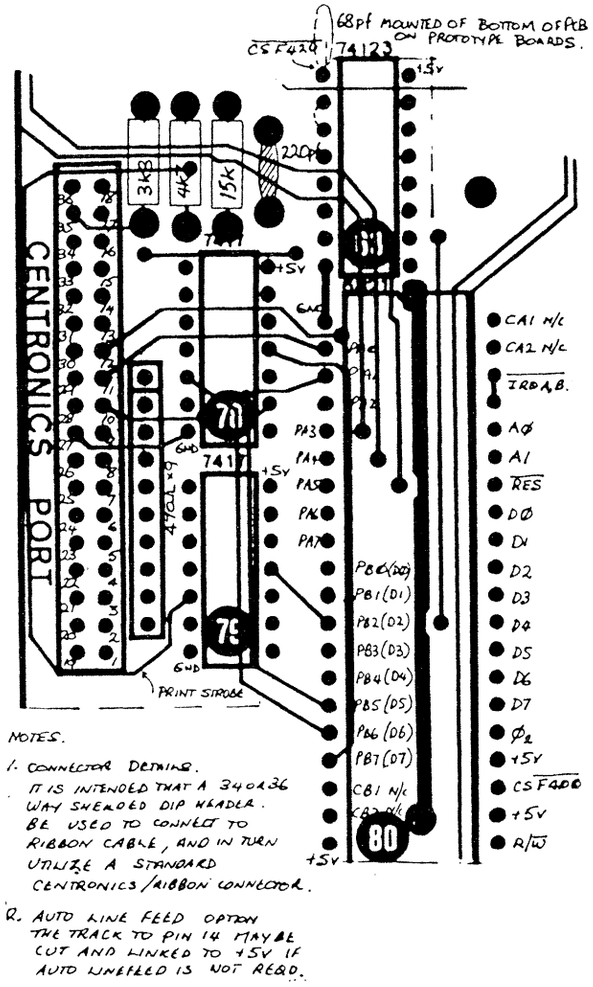
F403 04

Note the high bit of F401 and F403 may or may not be set.

Now write $FF to location $F402, then read it back again to ensure that the Port is latching the data. It should read $FF. If the data in the PIA is not correct, it may indicate a faulty PIA, which should be replaced, or that one or more of the control signals is not reaching the PIA, in which case the source of the control signal should be tested.

With your logic probe or CRO check that the reset line, pin 34 of IC 80, is high and that the data lines are all pulsing, ie the CPU data buss lines. If any of these are doubtful, check the equivalent line in the RAM section. This will indicate whether or not there is an open circuit track on the board. Ensure that the R/w line, the phase 2 clock, A0 and A1 are also present. Any missing or static signals should be traced back towards the CPU and repaired.

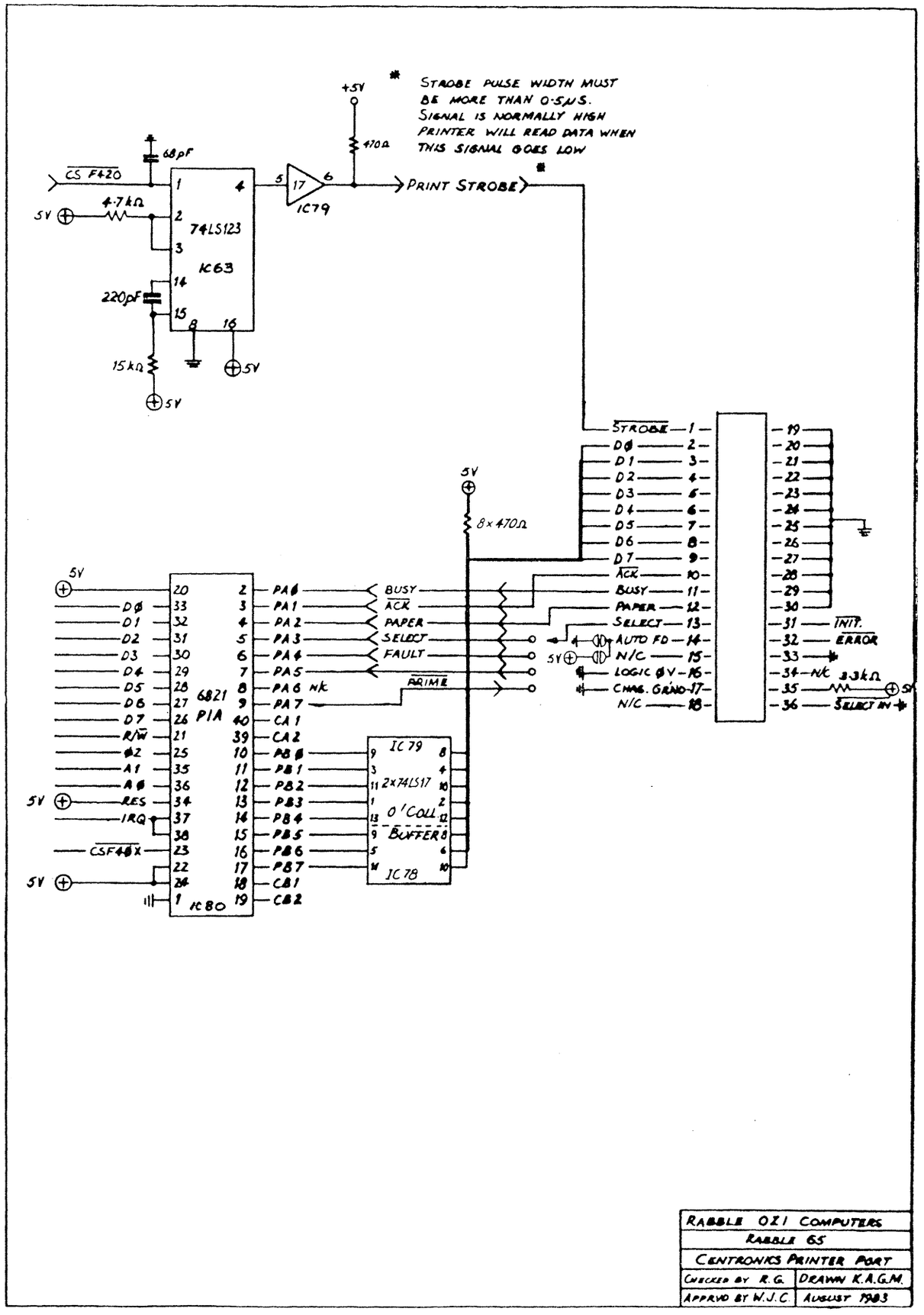
Finally check that the PIA is selected with a logic low pulse on pin 23 of the PIA, by performing a read or write to to the PIA at address $F40x.



NOTES.

1. CONNECTOR DETAILS.
   IT IS INTENDED THAT A 34 OR 36 WAY SHIELDED DIP HEADER BE USED TO CONNECT TO RIBBON CABLE, AND IN TURN UTILIZE A STANDARD CENTRONICS/RIBBON CONNECTOR.

2. AUTO LINE FEED OPTION
   THE TRACK TO PIN 14 MAY BE CUT AND LINKED TO +5V IF AUTO LINEFEED IS NOT REQD.



CHAPTER 9

FLOPPY DISC CONTROLLER
PARALLEL SECTION

ASSEMBLY

Fit IC sockets for IC's 89 - 92 and 109. Install the two resistor packs adjacent to the FDC connector, taking care to orientate the resistor pack correctly, pin 1 is marked with an indentation or spot at that end. The FDC connector should also be installed at this time. After all components are soldered into position , check all joints for solder bridges, missed pins etc., if neccessary clean away excess resin deposits.

The board is configured in manufacture to suit 8" mini floppies. If it is desired to use 5.25" mini floppies a number of track cuts and links need to be performed. The connections to the 50 way DIP connector for the FDC which require changing are as follows:-

INDEX pin 20 of the FDC connector is transferred to pin 24 of the connector.

DRIVE SELECT D is transferred from pin 32 to pin 22 for 5.25" operation. pin 22 is normally reserved for the READY line which is used on some drives and is not required for the Rabble 65.

MOTOR ON Pin 32 is connected to the motor control signal to provide control over d-c drive motors on 5.25" drives.

INDEX ENABLE is cut and linked as shown on the circuit to allow the d-c motor to accelerate up to normal operating speed before allowing the FDC to perform any data transfers to or from the disk. This change should always be carried out with the MOTOR ON change.

Each of these options is shown on the circuit and overlay diagrams opposite.

The connecting cable to either disk drive size should be via a 50 way cable. The connector on the 8" drives is a 50 way connector and the connections are pin for pin equivalent. The 5.25" drives have a 34 way connector to interface with the Rabble 65. To interface this drive, connect a 50 way cable as described for the 8" version, then prepare to connect the 34 way connector to the other end. The cable should be split between wire 16 and 17 at the drive end and pared back to allow for the number of drives being connected. The 16 wire side of the cable can be cut off, and the 34 wire side of the cable can be terminated on the 34 way socket for the 5.25" drive. All odd numbered connections of both ends of the cables of both sized drives are ground connections for the FDC and drive. Test that the cable and sockets are correctly orientated before

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connecting.

Once all connections and cables are completed, IC's 89 - 92 and IC 109 should be inserted into their respective sockets to complete the assembly of the parallel section of the FDC.

To change operation from 8" drives to 5.25" drives, a number of tracks need to be cut and links installed. The points where these alterations are made are highlighted on the printed circuit board by a circular pad, cut through the centre. Some of these pads have a link fitted during manufacture, others are open across the two halves. To cut a link use a sharp hobby knife and make two parallel cuts through the centre of the pad cutting across the link, and then lift the small section of track away from the board. To fit a link, carefully scrape away the solder resist on the two halves of the desired pad and then solder a short piece of wire across the gap.

The tracks affected by the different drive requirements are connected to :-

FDC PIN No.	8"	5.25"	No.Cuts / Links.
20	INDEX	IN-USE	2 / 2
22	READY	D.S.D	0 / 1
24	Not used	INDEX	0 / 1
32	D.S.D	MOTOR ON	1 / 1

CIRCUIT DESCRIPTION

The FDC contains four main sections. Briefly their functions are:-

1. PIA A 6821 peripheral interface adaptor. This device isused to control the mechanical movements of the disk drives and to inform the CPU of the status of the disk drives.

2. ACIA A 6850 asynchronous communications interface adaptor, is used to transmit and receive data to and from the disk drive as required by the computer. The ACIA also converts this data from eight bit parallel to serial format when writing to the disk, and from serial to parallel when reading from the disk.

3. DATA SEPARATOR The function of this section is to separate the data from the stream of pulses coming from the disk. A clock pulse is interleaved with each data bit which is stored on the disk.

4. MOTOR CONTROL This function is provided to save wear on the d-c drive motors of 5.25" disk drives. It is a timer network which activates the drive motors for about 3 seconds each time the FDC PIA is accessed. A delay is also inserted in the INDEX ENABLE line to provide motor speed to reach normal before data is read from the disk.

The data lines for both the ACIA and the PIA are in parallel. Their address locations are $C010 - C011 and $C000 - C003 respectively, decimal values for these locations are 49168 - 49169 and 49152 - 49155.

PB0 (Port B line 0), is the write gate. This gate, like all other signals in the FDC, is active low, ie the write gate becomes active or operational when the logic level of this gate is zero. The write gate when active switches the electronics in the disk drive ready to write data to the drive's head, hence the disk. However, the software for the FDC tests that the disk in the drive is not write protected. If it is write protected then the write gate is not changed and the electronics in the drive will remain in the read mode.

PB2, PB3. These are the direction and step lines that are used to position the head of the drive over the desired track of the disk. The stepping motor in the drive moves the head one position each time the step line is sent a low going pulse. The direction that the step motor drives the head is determined by the logic level on the direction line.

PB5, PA6 The PIA is organised to select one of four drives. This is controlled by PB5 and PA6 outputs, which are input to a 74LS139 to decode these two lines to provide four discrete drive lines. These lines each bufferred by a gate of a 7417, open collector buffer, and connected to the drives of the FDC connector cable.

PB6 This is the low current line which is used to reduce the write current to the head on the inner tracks of some 76 and 80 track drives. The electronics controlling the write current is contained in the disk drive itself and the low current brings it into operation if required.

PB7 HEAD LOAD, places the head assembly onto the disk media. When a drive has its drive motor running continuously, the raising of the head when not required to transfer data, significantly reduces the amount of wear on both the head and the disk.

All of port B and also PA6 of the PIA are configured as outputs to send control signals to the disk drive. Port A, with the exception of PA6, reads control information from the disk drive.

PA0, PA2, PA3 and PA4 are unused and their lines are tied low.

PA1 TRACK 00 is used to indicate when the head of the disk drive is positioned over the outermost track of the disk, which is track 00.

PA5 WRITE PROTECT goes low when the disk in the drive has been write protected. On 5.25" disks this is done by fitting an opaque label over the write protect indent on the side of the

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disk cover. On 8" disks the write protect is performed by removing the opaque label on the front edge of the disk cover. When this line is low the FDC is prevented from attempting to write to the disk.

PA7 INDEX / SECTOR is used on soft sectored disks to inform the FDC the precise angular position of the disk in relationship to that during the original write operation to the disk. The index pulse is generated once each revolution of the disk by an opto coupled device, looking through a hole in the cover of the disk and the disk itself as the hole rotates around to line up with these other holes.

PARALLEL SECTION FDC DEBUGGING

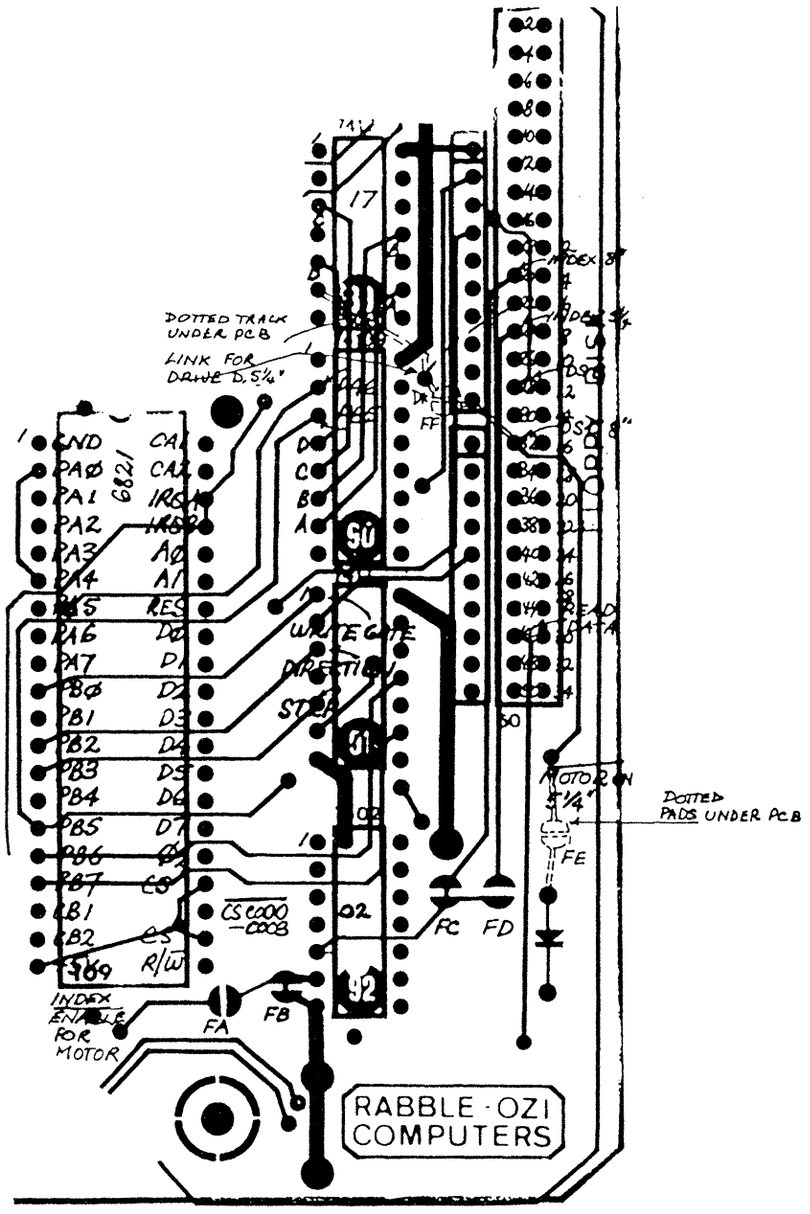
The parallel section of the FDC is a relatively simple stage of the Rabble 65, containing only five chips and a couple of resistor packages.

If it is suspected that a fault exists with this section of the FDC, test which of the functions are operable in the disk drive, controlled by the PIA, IC 109. If some functions operate then it is unlikely that the problem is within the PIA. Check all of the open collector buffers of the 7417's, IC's 89 and 91, to ensure that signals produced by the PIA are being output to the FDC connector.

If drives are not being selected correctly, then it is possible that IC 90, the 74LS139, could be at fault or that the drives may be internally configured to be a drive device number other than expected. Check that the selected drive output is being decoded correctly from the two inputs on pins 2 and 3 of the 74LS139. Outputs on this chip are on pins 4, 5, 6 and 7, which are then fed via the open collector buffers, IC's 89 and 91, to the FDC connector.

If nothing appears to operate correctly, check that all control signals are reaching IC 109, PIA. These are the CSC000, decimal 49152, for four consecutive locations on pin 23. Address lines A0 and A1 on pins 36 and 35 of the PIA. Check that all data lines are positively connected to the data buss, and that the R/w, and phase 2 clock signals are present.

If all appears well, initialise the PIA and alter the contents of the data registers, check that the data written into the output registers of the PIA are stored correctly. If this tests out correctly, then any fault must lie external to this section of the FDC. Refer to the serial section of the FDC for more information.

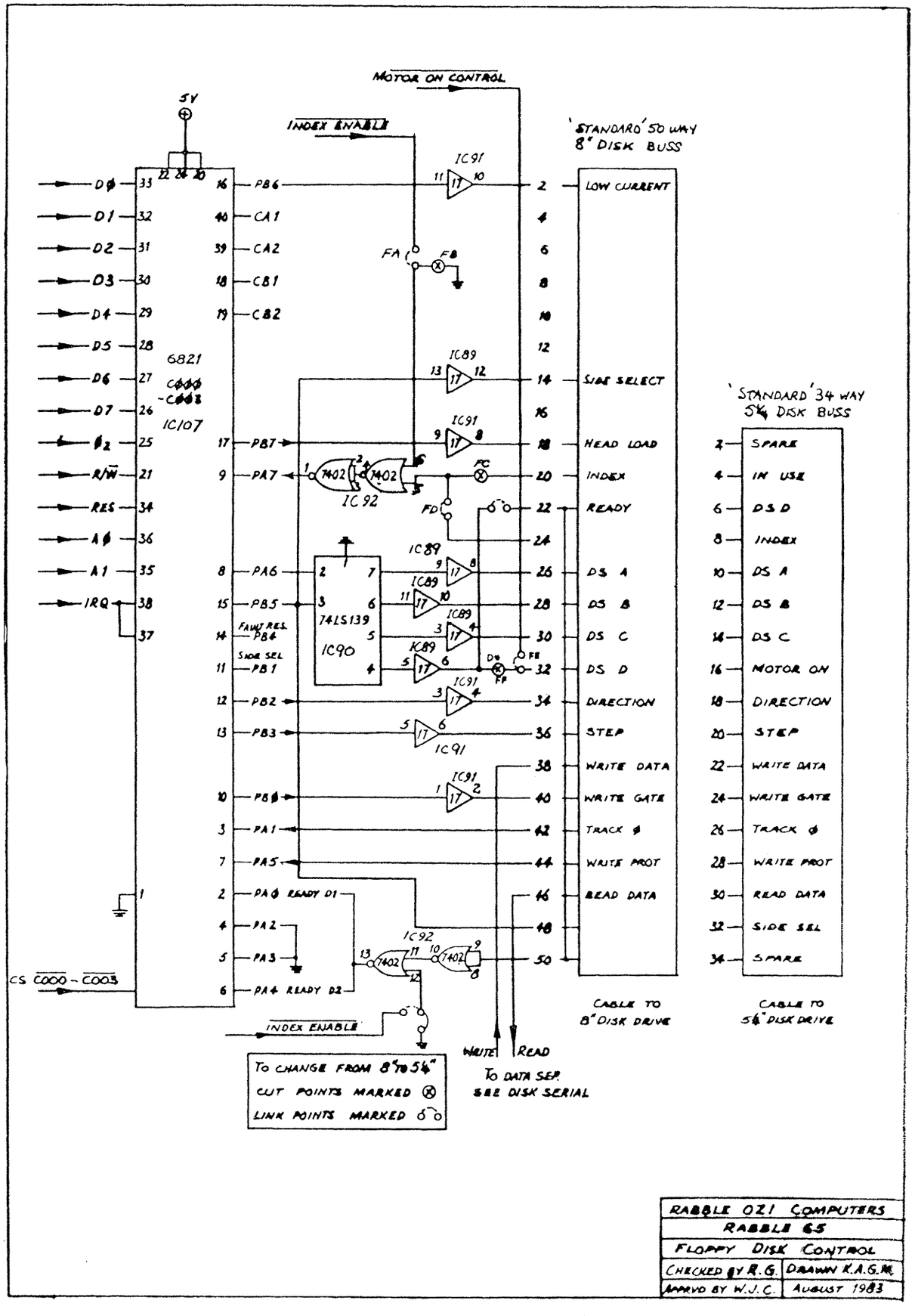


8" DISK SYSTEMS.

NO MODIFICATIONS ARE REQUIRED TO STANDARD BOARD.

5¼" DISK SYSTEMS.

1. REFER TO CPU CIRCUITS FOR CLOCK FREQUENCY TO SELECT 125 kHz.
2. CUT PADS AT FF
   LINK PADS AT FE
3. CUT PADS AT FC
   LINK PADS AT FD
4. CUT PADS AT FB
   LINK PADS AT FA
5. IF DRIVE SELECT D IS REQUIRED ON 5¼" LINK D* TO PIN 22 (PIN ON 5¼)' (A SHORT KYNAR WIRE JUMPER IS IDEAL)



RABBLE OZI COMPUTERS	
RABBLE 65	
FLOPPY DISK CONTROL	
CHECKED BY R.G.	DRAWN K.A.G.M.
APPVD BY W.J.C.	AUGUST 1983

FLOPPY DISK CONTROLLER
SERIAL SECTION

ASSEMBLY

Fit sockets for IC's 98 - 106 and 115 - 117, also fit the discrete components as shown on the component overlay. Take care with the orientation of the diode. After soldering in all components, once again check your work thoroughly and clean the board if neccessary.

The serial port is set up for 76 - 80 track drives during manufacture, but can be reconfigured for 40 track drives if neccessary.

All 8" drives are 76 or 80 track drives, standard 5.25" drives are 37 or 40 track drives. Some 5.25" drives are of a 96 track per inch density, and are a 76 or 80 track drive.

Should it be required to operate standard 5.25" drives, it will be neccessary to change the clock speed for the ACIA on the FDC serial port. This is done by cutting the track on the bottom of the board at pin 4 of IC 74, refer to the CPU section circuit diagram for this part of the circuit, and connect the isolated track to pin 3 of IC 74. This will provide a serial clock rate of 125KHz in lieu of 250KHz.

Note that conversion of the serial section of the FDC to standard 5.25" operation requires that simultaneous changes be made to the parallel section of the FDC.

Insert the nominated chips for this section and proceed to the serial circuit description to set up the six trimpots. It is essential to have access to a cathode ray oscilloscope with a bandwidth of at least 15MHz, to be able to set up the narrow pulse widths accurately.

CIRCUIT DESCRIPTION

The ACIA is, as stated earlier, used to convert parallel data to serial data and vice versa. The serial data is given a few extra bits of information, to provide a very high reliability factor. The ACIA is configured to provide eleven bits of information for each eight bit byte of data. The format of this data is:-

- one start bit
- eight data bits
- one even parity bit
- one stop bit

The serial clock rate is 250KHz for 76 - 80 track drives, in 8" and 5.25" formats. The standard 5.25" drive operates with a clock rate of 125KHz. Each 4uS a 250nS pulse is sent to the drive to be recorded on the disk. This is called the clock pulse, and is used as a means of keeping the data separator, on replay, informed of the exact timing of the disk,

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to maintain a high degree of accuracy. During recording, data pulses are sent to the disk only when the data bit is at logic one, otherwise no data pulse is recorded on the disk. The data pulse is identical to the clock pulse and is sent 2uS after the start of the clock pulse (if the data pulse is a logic one). Note that for the standard 5.25" drives, the times are doubled and the overall clock rate is halved.

The clock and data pulses are generated by a retriggerable one shot monostable, which is controlled by the 250KHz clock (125KHz for standard 5.25"). The pulse widths are adjustable to provide the ability to change between the two drive formats.

On reading information from the drive, the data stream contains a mixture of clock and data pulses, this is called raw data. A data separator is included on the Rabble 65 to recover the data only stream and feeds this to the the FDC ACIA. The separated clock signals are used to clock the data stream into the ACIA. Both these signals travel via pulse modifying networks contained in IC 100, a 74LS123.

The raw data from the drive is inverted and fed to the control gates of the separate clock and separate data outputs from the data separater. The output of the separate clock gate sets the 8602, IC 102, one shot by pulling pin 11 low, this sets the 2.9uS one shot. The 8602 output, pin 9 IC 102, goes low causing IC 105, 74LS00, pin 3 to go high and pin 6 goes low and inhibits the separate clock gate for 2.9uS, which is long enough to allow the next pulse, which is a data pulse if it is present, not to be seen at the separate clock output. However, the separate data gate input is ready to permit this pulse to be passed through as a separated data bit. At the end of the 2.9uS time period pin 6 of the 74LS00, IC 105, goes high again to enable the separate clock gate, whilst inhibiting the separate data gate. Since the interval between clock pulses is 4uS, the circuit is reset when the next pulse is seen.

As each data pulse is separated and fed to the separate data gate, the data pulse is fed to the other half of the 8602, IC 102, at pin 5. This triggers the 2.7uS one shot and the first stage of the 74LS74 flip flop, IC 103. If a clock pulse comes in after the data pulse, then both the one shot and the flip flops are reset. If no clock pulse is received at the end of the 2.7uS period, pin 7 of IC 102 goes high to set the clock input to the 74LS74, IC 103, flip flop at pin 11, and supplies the missing clock pulse to the 2.9uS one shot via the 74LS00 gates. Up to five missing clock pulses can be handled in this manner, whereupon the output of the 2.9uS one shot is reset. This condition is held until another pulse is input to the raw data input. The separate clock and data pulses are fed to the ACIA via a 74LS123, IC 100, which is used to stretch the width of the pulse. These conditioned signals are then fed to the ACIA. The ACIA uses the clock pulse to clock the data bit into its internal receive register, where these bits are assembled into parallel signals of eight bits ready for the CPU data buss.

SET UP INSTRUCTIONS

Setting up requires the use of an oscilloscope with at least a 15MHz

bandwidth.

There are six adjustments to be made to align the serial FDC. These are located immediately above the keyboard in a single row, numbering from left to right (1 - 6).

TRIMPOT	FUNCTION	5.25" PULSE WIDTH	8" PULSE WIDTH	PULSE POLARITY
1	Tx data	400nS	250nS	negative
2	Tx clock	400nS	250nS	negative
3	Rx clock	1.0uS	1.0uS	positive
4	Rx data	6.0uS	2.5uS	negative
5	Data sep.	5.4uS	2.7uS	negative
6	Data sep.	5.8uS	2.9uS	negative

The following is a description of the adjustments neccessary for 8" drives or high density 5.25", 80 track drives. Figures in brackets are for standard 5.25" drives only.

Adjustment of Tx Data Pulse and Tx Clock Pulse

1. Remove ACIA, PIA and 74LS00, IC's 115, 109 and 106. Handle carefully, using normal precautions for MOS devices.

2. Disconnect cable to floppy disk drive.

3. Connect CRO to pin 38 of the FDC socket, or to pin 2 of IC 101, 7417.

4. Adjust Tx data trimpot to obtain a negative going pulse width of 250nS, (400nS).

5. Ground pin 6 of the ACIA, IC 115, and adjust the Tx clock trimpot to obtain a negative going pulse widthe of 250nS, (400nS). These pulses will appear in the middle of the previous set of pulses so take care in watching which pulse you are adjusting.

Adjustment of Rx Clock Pulse

1. Feed the Tx pulses from pin 2 of IC 101 to pin 6 of IC 106, using a short length of Kynar wire inserted into the sockets, or soldered temporarily on the bottom of the board.

2. Connect the CRO to pin 3 of the ACIA socket.

3. Adjust the Rx clock to display a positive going pulse of 1uS, for all drives.

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Adjustment of Rx Data Pulse

1. Feed the Tx pulses from pin 2 of IC 101 to pin 8 of IC 106, using a short jumper.

2. Connect the CRO to pin 2 of the ACIA, IC 115.

3. Adjust the Rx data trimpot to obtain a negative going pulse of 2.5uS (6uS).

4. Carefully remove the links and replace the ACIA , PIA and 74LS00. Seal the position of the trimpots to prevent accidental rotation, with a suitable trimpot sealant. A small drop is enough.

Adjustments for the Data Separator

1. Connect pin 38 of the 50 way FDC connector to pin 46 of the same connector.

2. Connect the CRO to pin 9 of IC 102. Set the time base to 1uS/cm.

3. Adjust the extreme right hand trimpot to give a negative going pulse of 2.9uS, (5.8uS).

4. Remove IC 106, 74LS00.

5. Remove jumper installed in step 1 and install from pin 38 of the FDC connector to pin 8 of IC 106.

6. Connect CRO to pin 7 of IC 102.

7. Adjust the other Data Separator trimpot to provide a negative going pulse of 2.7uS, (5.4uS).

8. Remove the jumper and reinsert IC 106, 74LS00.

9. Seal the position of these two trimpots, to prevent accidental rotation of them.

This completes the adjustment of the serial section of the floppy disk controller.

DEBUGGING

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The serial section of the FDC contains an ACIA, for the parallel to serial and serial to parallel data conversion, a data separator, to separate the clock and data pulses, a number of pulse shapers and a disk drive motor controller for d-c driven drives.

The first test to carry out in the event of malfunction, is to ensure that the FDC clock is present. This is a 250KHz clock pulse, (125KHz for 5.25") and it appears on pin 4 of IC 115, the ACIA, and also on pins 2 and 9 of IC 98, 74LS123. Test the ACIA to ensure the eight data lines are connected to the data buss. Test also for control signals, phase 2 clock on pin 14 of the ACIA, the R/w line on pin 13, and the address line A0 on pin 11. Monitor pin 9 of the ACIA with a logic probe or CRO to ensure a low going pulse appears when a read or write operation is performed to address location $C010, decimal 49168.

Write to the ACIA at $C010, after initialisation, and ensure that data is output in serial format on pin 6 of the ACIA, IC 115. Reading of data by the ACIA can only be performed if data is input from the disk and the data separator is functioning correctly.

Test IC's 98 and 100, 74LS123's, by performing the set up adjustments described at the end of the circuit description. The same applies to IC 102, 8602, for the data separator.

Check the serial data chain from pin 6 of the ACIA, through the gates of IC 99, 74LS00, to IC 101, 7417. Check that the Tx clock appears on pins 5 and 13 of IC 99, 74LS00.

To check the read data function, ensure that a data signal is being input to the data separator. This will appear on pins 1 and 2 of IC 106, 74LS00. Ensure that the timing adjustments of IC 102, 8602, are correct for the disk drive being used. Refer to the set up instructions if neccessary. Follow the pulse train from IC 106, pin 3 through to pin 6 and onto pin 5 of IC 102, pin 3 of IC 103 and also pin 2 of IC 105. If the 8602 output from pin 9 is functioning correctly, an output will be available at pin 3 of IC 105 and also on pin 6 of the same chip. An inverted signal should be present at pin 10 of IC 106 to produce the separated data signal at pin 8 of IC 106.

It is difficult to test the 74LS74 flip flops, as they require missing clock pulses to function. Test that the flip flops are being reset by monitoring pins 1 and 13 of both IC's 103 and 104. Check that IC 103 is receiving data pulses on pin 3 and that the output on pin 6 is also switching. If the other sections of the 74LS74's are suspected of malfunctioning, then it is recommended to test by substituting a known good chip into IC locations 103 and 104.

Test that the separated data pulses at pin 2 of IC 100, 74LS123, produce output pulses at pin 4, with a pulse width of 2.5uS (6.0uS). If neccessary adjust the Rx data pulse trimpot as described in the setup instructions. Check that the separate clock signals at pin 9 of IC 100 are triggering the monostable to produce pulses at pin 5 of IC 100. These pulses should be 1.0uS wide for all systems. Ensure that both these signals appear at the ACIA pins 2 and 3 respectively.

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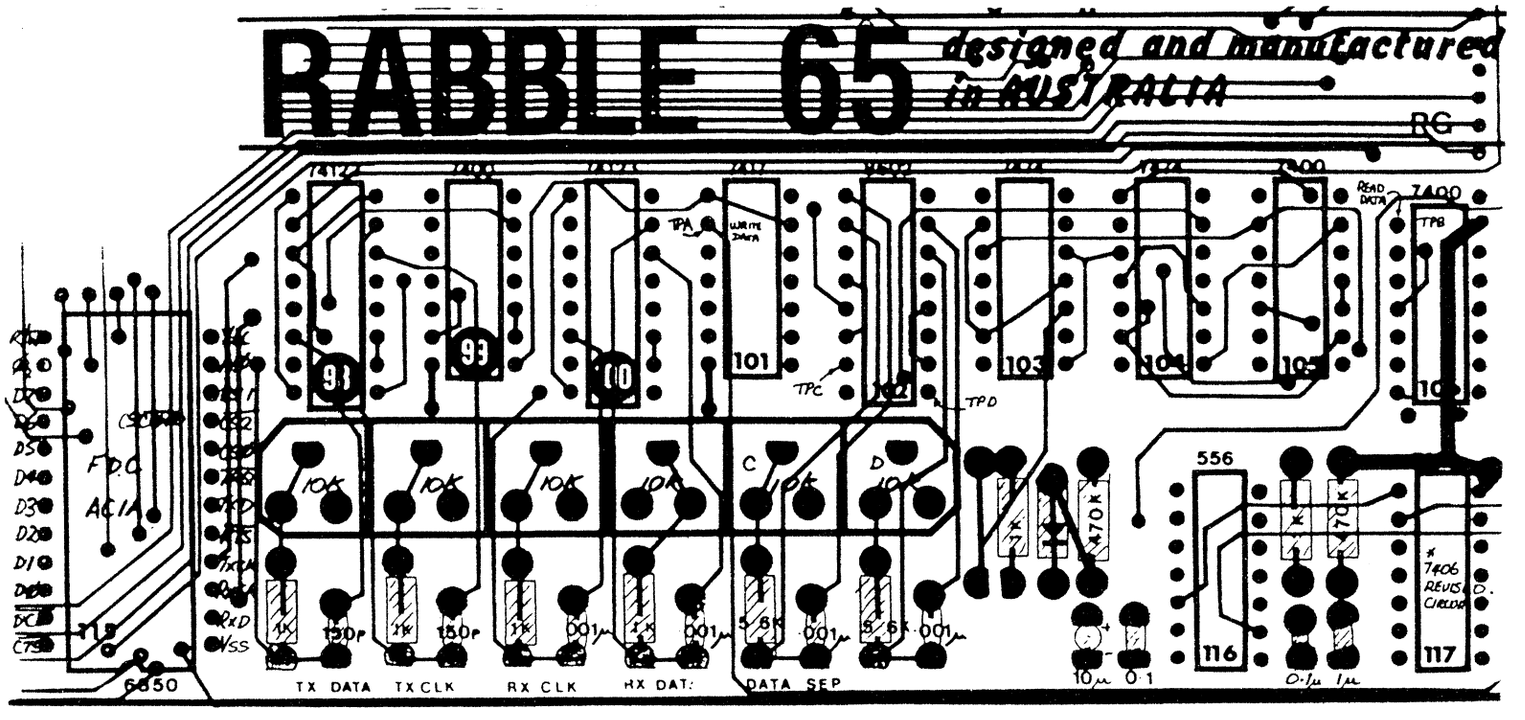
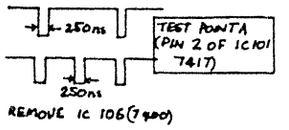
The motor controller is activated by accessing address $C000, which should provide a negative going pulse to pin 6 of IC 116, NE556, via the open collector invertor gates of IC 117, 7406. The output of the first half of the NE556, pin 5 should go high for about 3 seconds. This output is inverted by another gate of IC 117, 7406, pin 1 input and pin 2 output. The low going signal is R C coupled to pin 8 of IC 116, NE556, and a negative going pulse should be evident at this point. The output on pin 9 will go low about 500mS after $C000 is accessed. This output is called the index enable, and is used to permit access of the index sector line to the PIA in the parallel section of the FDC. The motor controller is not wired in the standard system, therefore, ensure that your system has been configured for it prior to attempting repairs.



ADJUSTMENT PROCEDURE FOR FLOPPY DISK CONTROLLER. (SHORT CHECK LIST)

1. REMOVE IC 115 6850 AND IC 107 6821
2. ADJUST TX DATA TO GIVE 250ns (400ns FOR 5¼)
3. GROUND PIN 6 OF ACIA IC 115
4. ADJUST TX CLOCK TO GIVE 250ns (400ns FOR 5¼)



FDC CONN. 5. CONNECT PIN 38 (WRITE DATA) TO PIN 9 OF IC 100 (74123) REMOVE IC 106 (7400)

6. ADJUST RX CLOCK TO GIVE 1µs PW GOING ON PIN 3 OF ACIA (6580, IC 115)

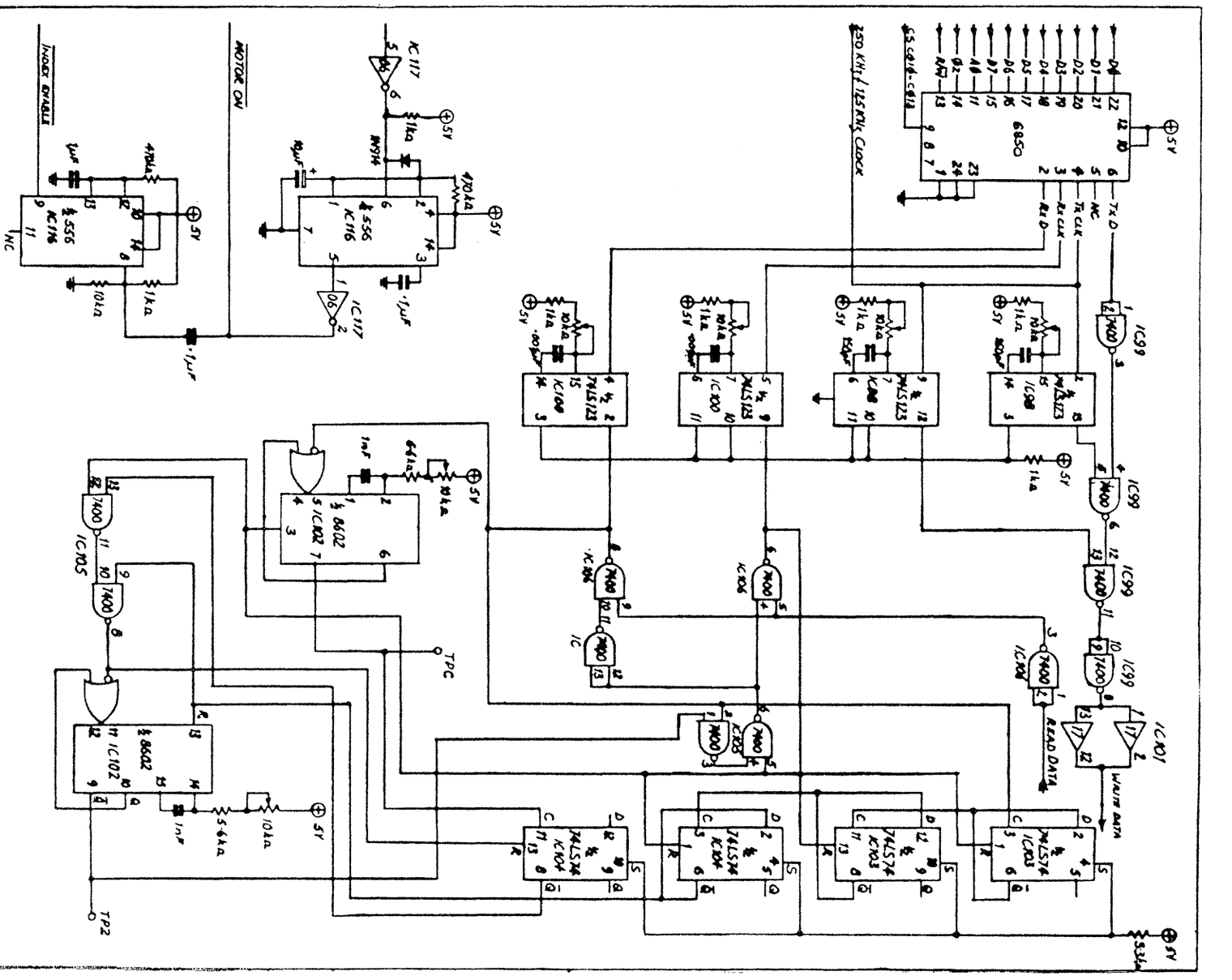
FDC CONN. 7. CONNECT PIN 38 (WRITE DATA TO PIN 2 OF IC 100 (74123)

8. ADJUST RX DATA TO GIVE 2·5µs NEGATIVE GOING ON PIN 2 OF ACIA (6·0µs FOR 5¼)
9. REPLACE IC 106 (7400)

DATA SEPERATOR ADJUSTMENT (SHORT CHECK LIST)

10. CONNECT PIN 38 (OF FDC CONNECTOR) TO PIN 46 (OF FDC CONNECTOR)
11. ADJUST DATA SEP POT D TO GIVE 2·9µs NEGATIVE PULSE ON TPD (PIN 9 OF IC 102) (5·8µs FOR 5¼")
12. CONNECT PIN 38 (OF FDC CONNECTOR) TO PIN 5 OF IC 102 (8602) ADJUST DATA SEP POT C TO GIVE 2·7µs NEGATIVE PULSE ON TPC (PIN 7 OF IC 102) (5·4µs FOR 5¼")
13. REMOVE ALL LINKS USED, REPLACE 6850, 6821

NOTE: ALL ADJUSTMENTS ARE CRITICAL AND SHOULD BE CARRIED OUT BY SOMEONE EXPERIENCED WITH OSCILLOSCOPE OPERATION



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CHAPTER 10

16 / 18 PIN I/O BUSS

ASSEMBLY

The Rabble 65 16/18 pin I/O buss uses five chips to provide four I/O busses. Assemble this section by installing IC sockets for IC's 26 and 43 - 46. Fit 18 pin sockets to the four I/O busses. Solder these sockets in carefully, and then inspect the board for any solder slivers or other defect, clean board if neccessary.

Install the relevant IC's as shown on the component overlay to complete the assembly.

CIRCUIT DESCRIPTION

Provision is made for four 16/18 pin I/O busses on the Rabble 65 computer. Each of these can support upto 7 ACIA's, 3 PIA's or a single VIA. These devices are connected to the I/O buss via an 18 pin DIP header plug and connecting cable. The buss permits the user to select I/O devices of their own choosing in serial or parallel format. Some of the devices currently available for operation from these ports include an EPROM programmer, programmable sound generator, speech generator, high resolution colour video board, printer interface and a prototyping breadboard. New peripheral designs are constantly being produced and are released from time to time.

Each of the 16/18 pin I/O busses occupies 16 memory locations.

I/O buss No.	1	$C700 - $C70F	decimal 50944 - 50959
	2	$C710 - $C71F	50960 - 50975
	3	$C720 - $C72F	50976 - 50991
	4	$C730 - $C73F	50992 - 51007

The address blocks are decoded by IC 46, 74LS138. This chip is a 1 of 8 decoder, which is enabled by the CSC7xx line from IC 66, pin 7, also a 74LS138, and address line A7 being low. The outputs of IC 46 are then selected by the address lines A4, A5 and A6, to provide eight blocks of sixteen bytes. Only the first four of these blocks are utilised on the Rabble 65 for the I/O buss. These I/O select lines are inverted by IC 45, 74LS04,to provide a high select input to IC's 26 and 43. The non inverted CS lines are also fed directly from the IC 46 outputs, to pin 9 of the related I/O buss socket.

IC's 26 and 43, 74LS08's, are quad dual input AND gates. Each of these gates AND's a CS line with an address line A2 or A3 to provide an output LA2 or LA3 respectively, to the appropriate I/O buss. The chip selected address lines are included in this model to maintain compatibility with older systems, which operated with only a 16 pin buss. These systems

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did not provide a separate chip select output to enable the peripheral attachment. These older peripherals will still operate normally with the Rabble 65. Simply insert the 16 pin plug into the 18 pin socket of the CPU board using the 16 pins closest to the Centronics port socket.

IC 44, 74LS245, is an octal three state transceiver. This chip is enabled by the CSC7xx line connected to the enable input, pin 19. The transceiver is used to transfer data to and from the I/O buss, whilst maintaining a high degree of immunity from the peripherals when not in use, and providing good drive capabilities when selected. The direction of data flow is controlled by the R/w line connected to pin 1.

When the CSC7xx line is high the transceiver goes into the high impedence state and no data is transferred in either direction. At the same time, however, there is no I/O buss selected.

Other lines connected to the I/O busses in parallel are the R/w line, phase 2 clock and address lines A0 and A1.

Power supply rails of +5 volts and ground are also available to permit the driving of peripheral devices directly from the Rabble 65 power supply. Current drawn from these sockets should not exceed 250mA. Larger currents may cause overheating of the sockets and also result in poor regulation of the supply rail at the peripheral board. Keep interconnecting cables as short as practicable.

DEBUGGING

To locate faults on this section of the Rabble 65 board, or to test this section, disconnect all peripherals plugged into the I/O buss. This is to prevent a faulty attachment from reflecting into the area under test. If the removal of the I/O device clears the fault then the problem is most likely within that device.

First test in fault location is to ensure that the chip select lines are being decoded correctly by writing to each I/O buss and observing with a logic probe on pin 9 of each I/O buss that a low going pulse is received. Check also that the R/w line, phase 2 clock and address lines A0 and A1 are present on pins 2, 3, 4 and 5 respectively. These latter pins are in parallel on all four sockets.

Test pin 19 of IC 44 to ensure that the transceiver is being enabled when any of the I/O busses are being accessed. Ensure that the R/w line is reaching the same chip on pin 1.

Write some data to an I/O port, and watch for this data on pins 1 and 11 - 17 of the I/O busses. Check both sides of the transceiver, IC 44, if any doubt exists about data reaching the I/O busses.

Check the CS lines from IC 46, 74LS138, pins 15, 14, 13 and 12, follow these through IC 45, 74LS04, to ensure that these CS lines are inverted. At the outputs of IC 45 the CS lines will normally be low and will go high when the appropriate block is accessed. Next check that LA2 and LA3 are activated correctly, by writing to the I/O buss selected,

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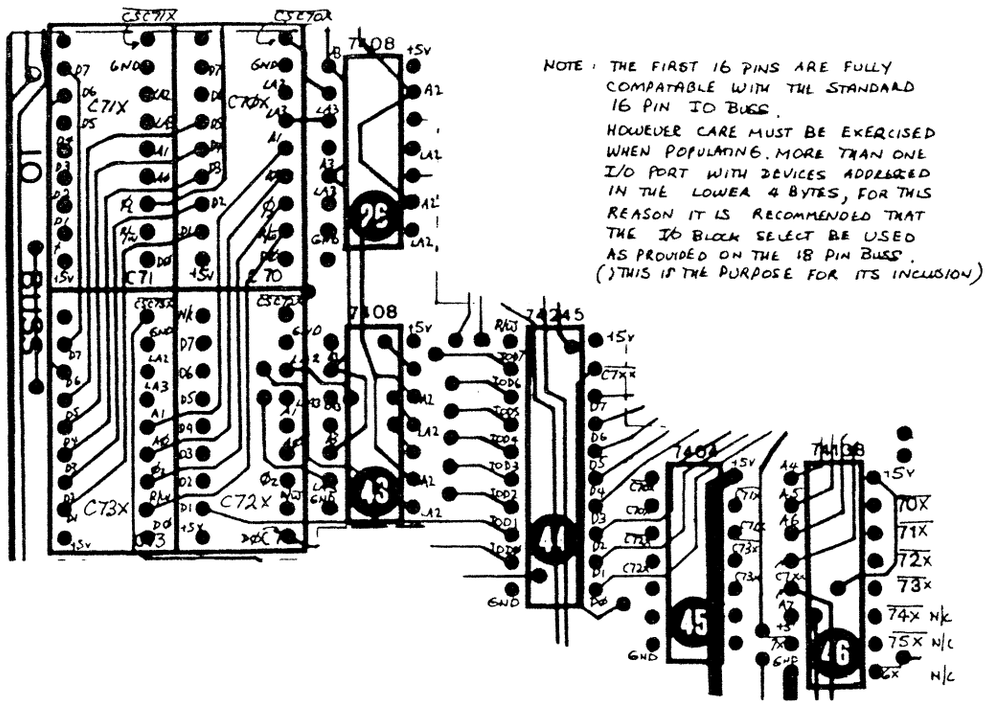
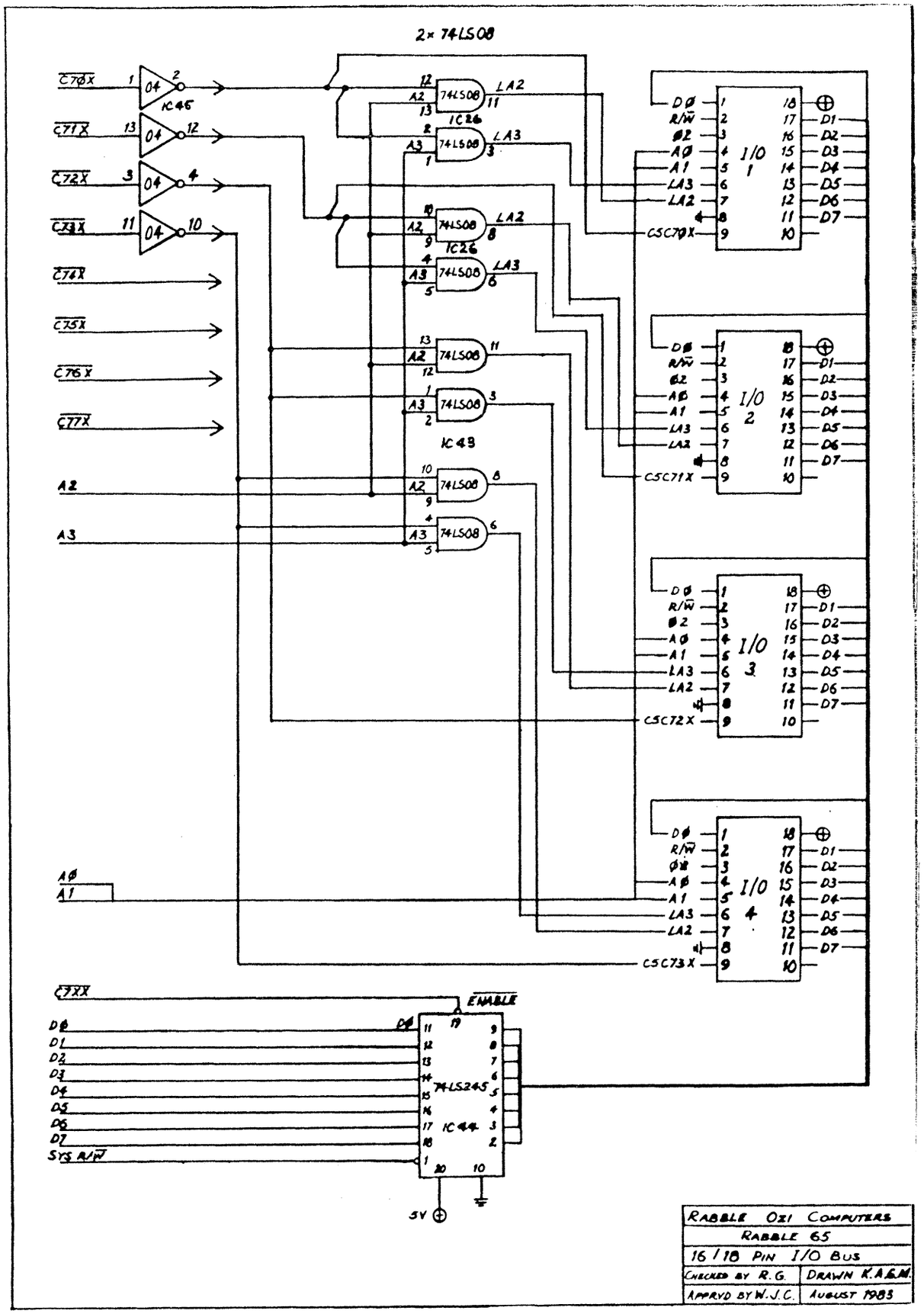
base address plus four for LA2 and base address plus eight for LA3. For example, to test LA3 for I/O buss No. 2, we take the base address of $C710 plus 8, and come up with $C718. Therefore to test LA3 on buss No. 2, a read or write to $C718 will cause a positive going pulse to appear on pin 6 of I/O buss No. 2.

This tests the I/O buss out. If any fault exists after the I/O device is reconnected, it is possible that there is insufficient power supply filtering on the I/O device, which is reflecting back to the Rabble 65. Excess loading of the A0 and A1 lines, the phase 2 clock and the R/w lines can also produce indeterminate effects on the system. Refer to your peripheral attachment manual for further assistance.



NOTE : THE FIRST 16 PINS ARE FULLY COMPATABLE WITH THE STANDARD 16 PIN IO BUSS. HOWEVER CARE MUST BE EXERCISED WHEN POPULATING. MORE THAN ONE I/O PORT WITH DEVICES ADDRESSED IN THE LOWER 4 BYTES, FOR THIS REASON IT IS RECOMMENDED THAT THE IO BLOCK SELECT BE USED AS PROVIDED ON THE 18 PIN BUSS. ( )THIS IS THE PURPOSE FOR ITS INCLUSION)



RABBLE OZI COMPUTERS	
RABBLE 65	
16/18 PIN I/O BUS	
CHECKED BY R.G.	DRAWN K.A.&M.
APPRVD BY W.J.C.	AUGUST 1983

CHAPTER 11

RAM

The Rabble 65 uses 6116LP3 2K x 8 static RAM chips for its read write memory. This RAM is used by both the system memory and the video display memory. The video display uses 2K of the total available 52K of RAM provided for on the board. This leaves 50K of RAM for use by the CPU and the users programmes, of which 48K is contiguous and the other 2K is separated to provide a BASIC protected area for user machine code programmes.

The 2K RAM chips used throughout this computer are of a CMOS construction and due care should be excercised in their handling. A maximum of 25 of these chips can be installed to provide the 50K of RAM. The major portion of RAM is located from address $0000 through to address $BFFF, 48K. The other 2K is located from $C800 to $CFFF.

Each chip has 24 connections, of which there are 11 address lines, 8 data lines, a chip select, chip enable, a read / write line and two power lines.

The address lines are connected to the CPU, which is constantly setting up these lower order addresses. The same address location in each chip is specified, but not activated until the chip select line of a chip is activated.

To activate a chip select (CS) line, the high order address lines are decoded by a group of 74LS138's which will select any 2K block of RAM during the period which the phase 2 clock is high. This selected block of RAM has its data lines connected to the data buss and then information is transferred to or from the chip, according to the status of the read / write (R/w) line. If the line is high, data is read from the RAM chip and if low data is written to the RAM chip.

RAM Stage 1

ASSEMBLY

This stage of assembly deals with the lower 16K block of RAM and the required decoding.

Install sockets for IC's 8, 22 - 25 and 39 - 42. Solder each pin of each socket carefully, ensuring that no pin is left unsoldered and that no solder blobs or slivers exist. The tracks on this area of the board are extremely close, and great care should be excercised.

Insert IC 8, 74LS138 and IC 25 6116LP3. Do not fit any other RAM chips until the first chip has been proven to work correctly. The RAM chip, the 6116, is a CMOS device, and as such the usual safety

precautions for CMOS devices should be observed.

If the monitor ROM, video, keyboard and CPU sections have been completed, apply power and press the RESET key. The screen should display a short message "Insert disk in drive A and press return". This indicates that at least some of your memory is working. At this point, key in a memory test programme and test locations from $0300 - $07FF, to prove the first chip as satisfactory. Testing memory locations below $0300 may cause the system stack pointers and programme to be overwritten and thus cause the programme to crash.

Once the first chip has been proven, fit the other chips into their respective sockets. Once again test this new memory with a memory test programme to ensure that all is well.

If less than the full 16K of RAM is being installed, then fit the 6116 chips into the available sockets in the following order, 25, 42, 24, 41, 23, 40, 22, 39.

CIRCUIT DESCRIPTION

The eight RAM chips are selected individually, as required by the decoding of the upper level address lines, A11 - A15, after buffering from the CPU. Address lines A14 and A15 are used to enable the 74LS138, IC 8, when these lines are both low. This indicates that a memory location in the lowest 16K block is to be selected. Address lines A11, A12 and A13 are then decoded to select an output according to the input. The outputs are normally high, and when the particular output is selected, the level shifts to a logic zero. This signal is applied to the corresponding CS and OE, pins 20 and 18, of the 6116LP3 RAM chips.

When the RAM chip is selected, the address inputs are enabled on that chip to select one of the 2048 discrete memory locations. The R/w line determines which direction the data transceiver is going to pass data.

The RAM chips are wired in parallel with each of the other RAM chips, with the exception of pins 18 and 20. These pins of each individual chip are connected together, and the resultant line, one for each memory chip, is connected to the address decoding chip output relevant to that chip. This line is called the chip select line (CS).

The CS line decoding is all referenced to the timing of the phase 2 clock. The 74LS138 is not enabled until after the phase 2 clock signal has reached a logic one lavel.

DEBUGGING

Any fault in the RAM section should be isolated to a specific 2K block or number of blocks, with the use of a memory test programme.

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The offending 2K block should be inspected visually to ensure that the 6116 is seated in the socket correctly and that none of the tracks to the chip are open circuit, including solder connections to the socket. Next ensure that the chip is receiving its CS signal by looking at pin 18 or 20 of the appropriate chip and performing a read or write operation to that address block. To assist in calculating the address blocks, two digits appear at the pin 24 end of each of the RAM chips which indicate the high order address bits for that chip, eg IC 40 shows " 28 " at the pin 24 end of the chip. This means that the base address for that chip is $2800.

If all memory appears to be defective, and the system will not start up after power on or reset, it is probable that an address line or data line is shorted to another line, to ground or to the supply rail. In this case check all lines of the address and data buss, by metering each line with each other line and the supply rails to ensure that no shorts exist. Inspect each individual track to ensure that no open circuit is causing the problem. Test that the phase 2 clock and the R/w lines are being activated at the chip.

A faulty 6116 may also cause the problem, and if suspected, remove all RAM except for IC 25. Test the memory again, and if OK then the fault lies in one or more of the removed chips. If still faulty, remove IC 25 and replace with one of the other RAM chips. Test again, if OK start replacing chips in groups, with the power off, and test each group as it is inserted.

If the fault still exists the problem may lie elsewhere in the CPU system. Check that the video display is functioning correctly, also the CPU and, the keyboard and ROM sections.

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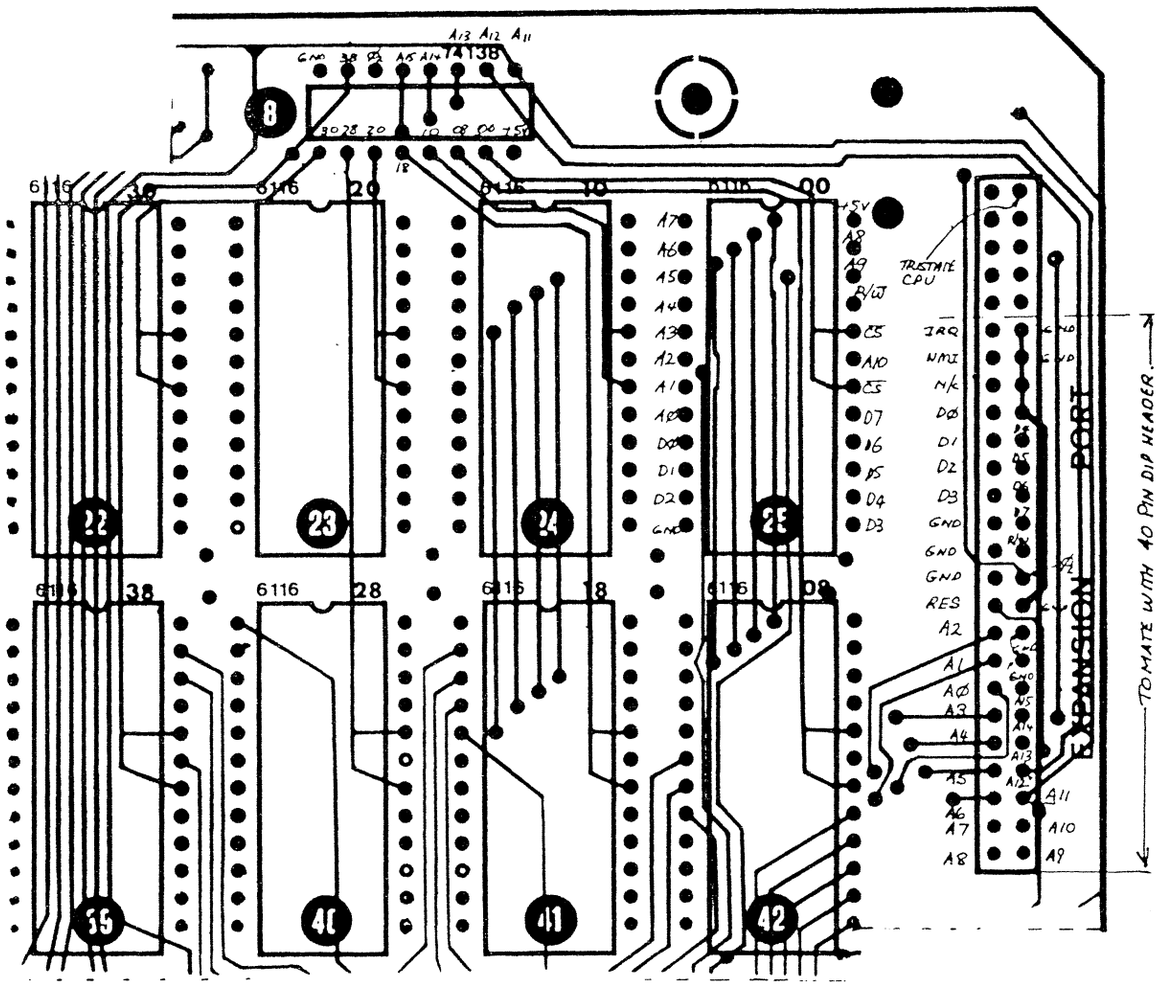

RABBLE 021 COMPUTERS	
RABBLE 65	
R.A.M. I	
CHECKED BY R.G.	DRAWN K.A.G.M.
APPROVED BY W.J.C.	AUGUST 1983

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RAM Stage 2

ASSEMBLY

To make use of this next 16K block of memory, it is assumed that the first 16K of RAM has been fully populated to provide contiguous memory.

Solder into position IC sockets for IC's 6, 7, 18 - 21 and 35 - 38. Check over as detailed in RAM stage 1.

Insert IC's into their respective sockets, and perform a memory test to ensure that the old memory as well as the new memory is functioning correctly.

CIRCUIT DESCRIPTION

The same address lines are used to decode this section as are used in stage 1, however, the address line A14 is inverted by IC 7, before going to the decoder chip IC 6, 74LS138. This line, A14 high, together with A15 low, and the phase 2 clock signal enables the decoding chip IC 6, when any of the addresses in the range of $4000 - $7FFF appears on the address bus. 2K blocks are decoded by the use of address lines A11, A12 and A13 applied to the address inputs of the 74LS138 decoder.

Outputs from the decoder chip are connected to the relevant CS pins of the 6116LP3 RAM chips.

The RAM connections are identical to that described in stage 1, with the exception of the CS lines which come from IC 6 instead of IC 8.

DEBUGGING

Ensure that IC's 6 and 7 are functioning correctly. IC 7 is a 74LS04 inverter, used to invert the A14 address line logic, and this inverted A14 line is connected to pin 5 of IC 6, 74LS138. Check that address lines, A11, A12, A13 and A15 are reaching the decoder chip, as well as the phase 2 clock signal. If all checks normally, then write to each address block within the 16K block in turn and ensure that the CS line is reaching pins 18 and 20 of the appropriate 6116 RAM chip. If a fault still persists, run a memory test programme as described in stage 1, to locate the offending RAM chip. Replace as neccessary.

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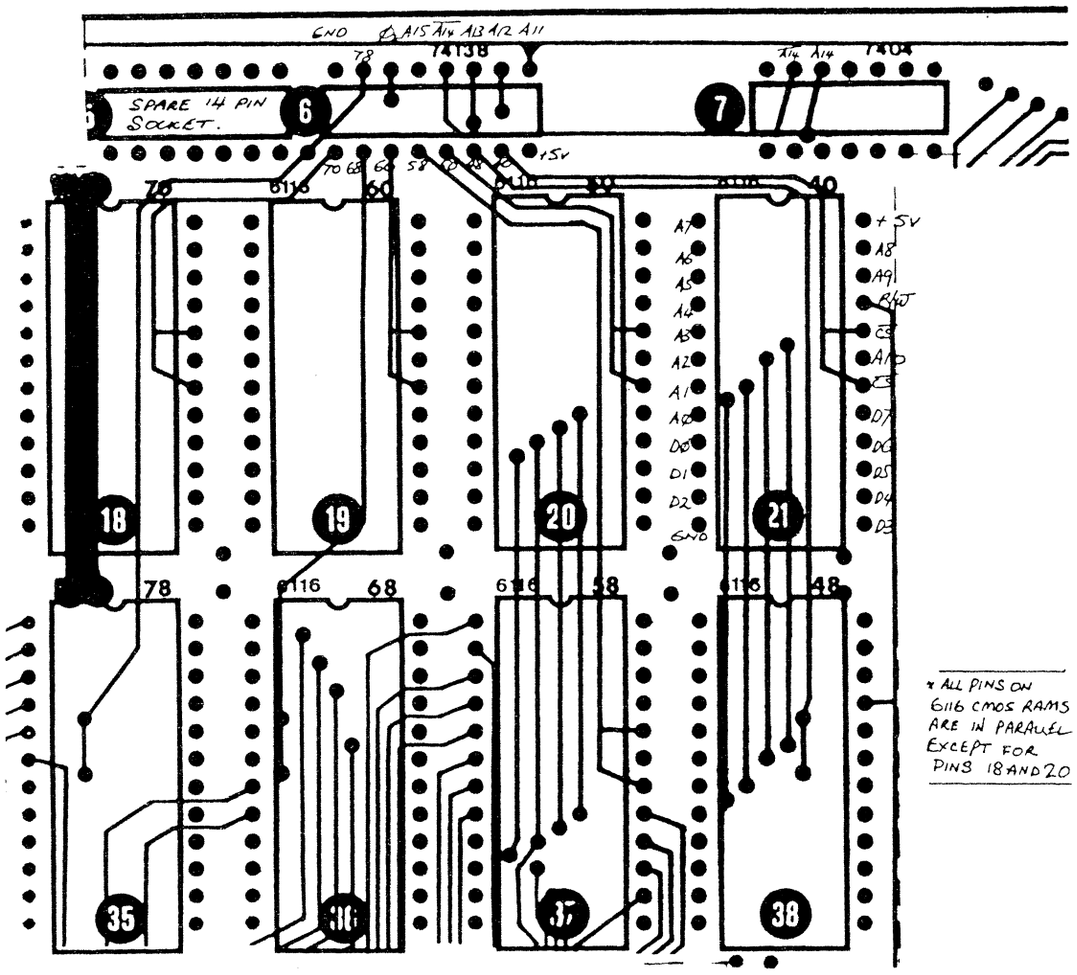
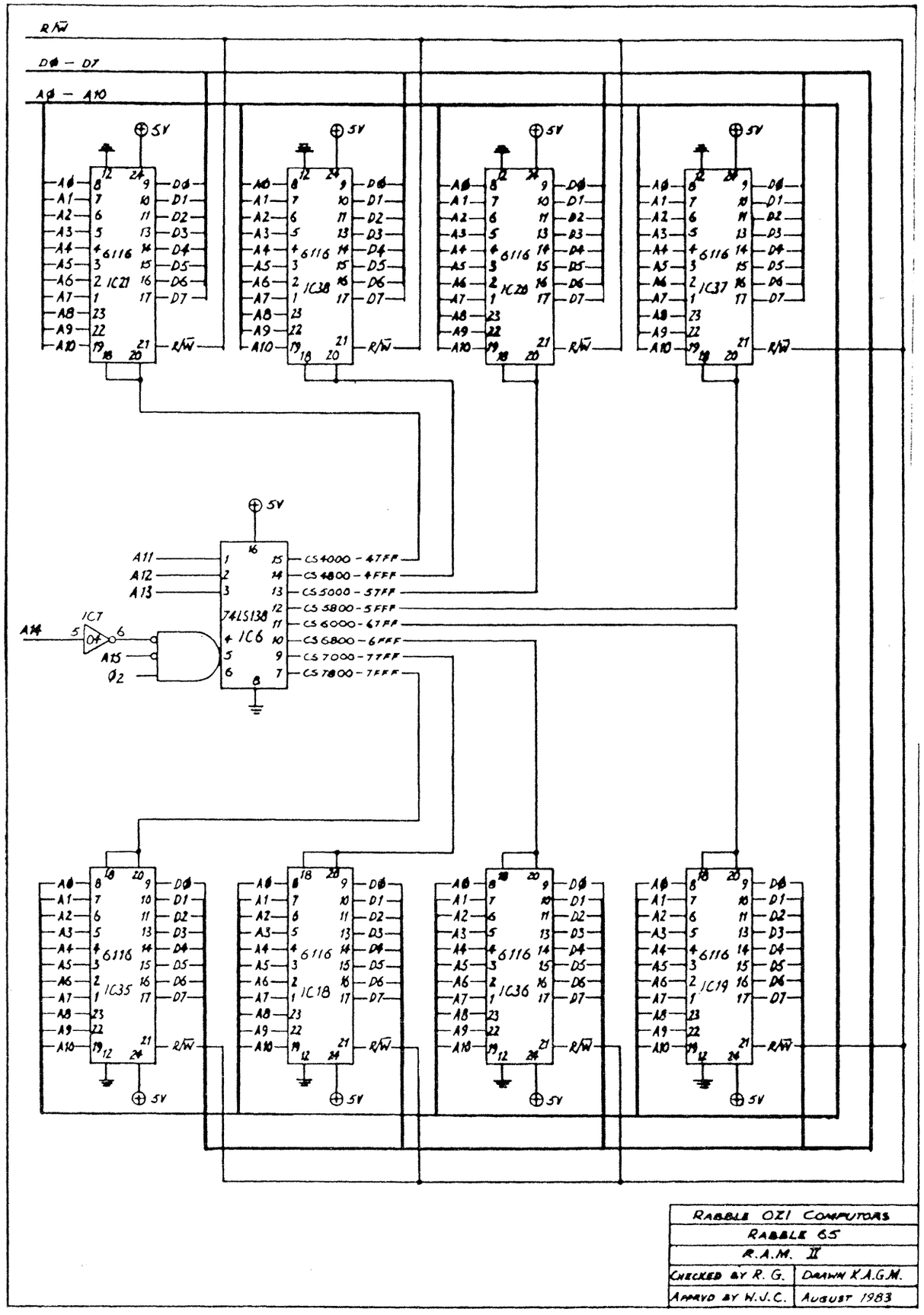




RABBLE OZI COMPUTERS	
RABBLE 65	
R.A.M. II	
CHECKED BY R. G.	DRAWN K.A.G.M.
APPROVED BY W.J.C.	AUGUST 1983

RAM Stage 3

ASSEMBLY

Thirteen chips are involved with this stage, these are IC's 1 - 4, 14 - 17 and 30 - 34. IC 30 provides a 2K block of memory at address locations starting at $C800, whilst the rest of the memory provides a 16K block which is contiguous to the previous block. Insert IC sockets for IC's 1 - 4 and the required RAM chips. Check work as detailed in stage 1.

Insert IC's 1 - 4 and check address lines A11 to A15, then test that CS line outputs from the 74LS138's are being selected correctly. When satisfied all is well, insert the required RAM chips and run your memory test programme.

CIRCUIT DESCRIPTION

The third, 16K block of RAM is decoded by IC 2, 74LS138, in a similar manner as stages 1 and 2. The differences with this chip are that the A14 line is true as in stage 1 and the A15 line is inverted.

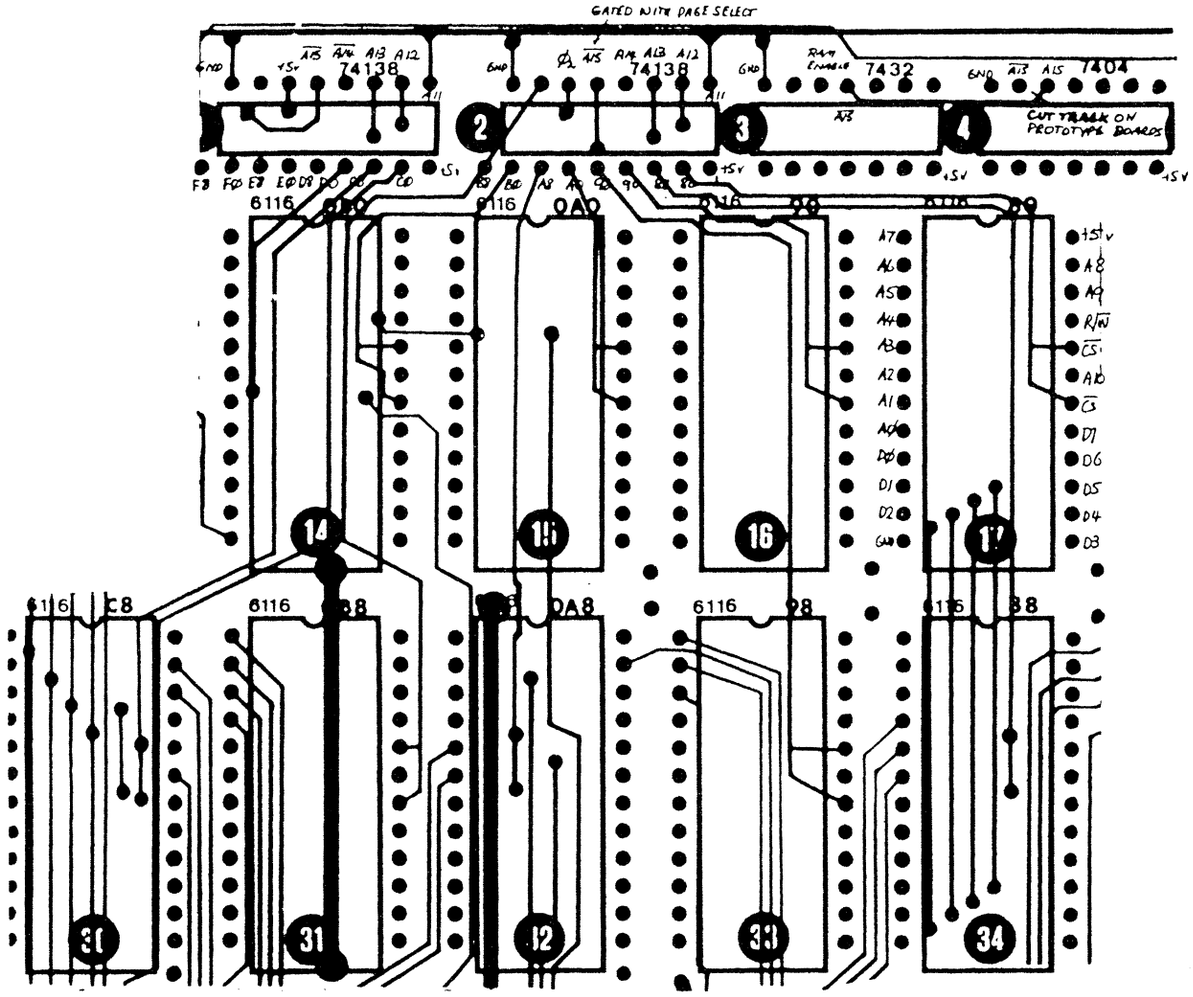
A15 is ORed prior to the decoder chip IC 2, to provide for page swapping. The chip used for this purpose is a 74LS32, IC 3. The other input comes from the page swapping section described in the ROM chapter.

The 6116 RAM chips are organised in the same manner as the previous two stages.

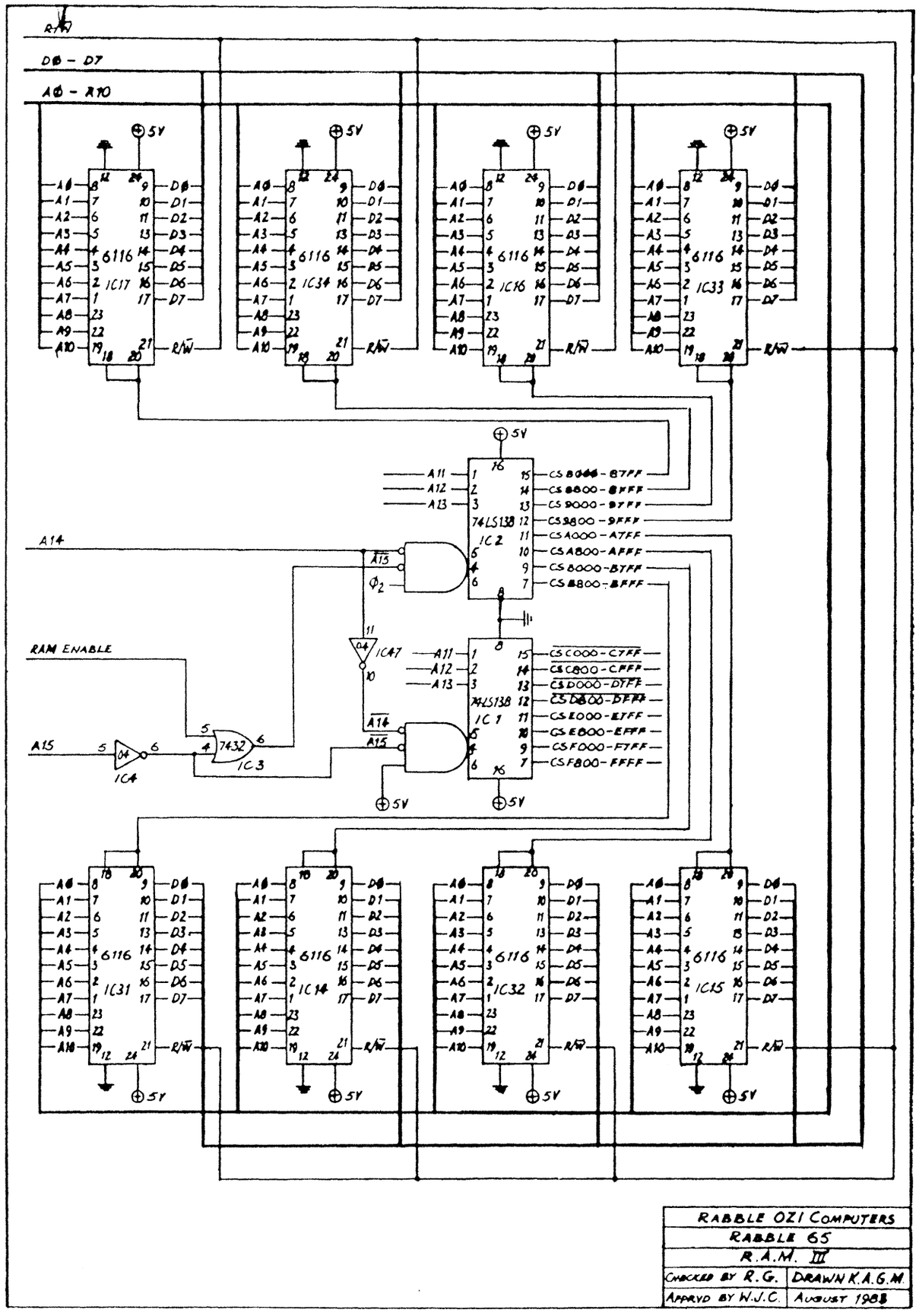
DEBUGGING

Ensure that A14 and A15 address lines are passing through the gating of IC's 3 and 4, 74LS32 and 74LS04. Check that all address lines A11 through to A15 and the phase 2 clock are input to IC's 1 and 2, 74LS138's. Then check that the decoded outputs from these chips are correct and are reaching their respective RAM chip select lines on pins 18 and 20.

RAM faults should be handled in the same manner as described in stage 2.



NOTE IC30, 6116 IS NOT SHOWN ON CIRCUIT DIAGRAMS.



RABBLE OZI COMPUTERS	
RABBLE 65	
R.A.M. III	
CHECKED BY R.G.	DRAWN K.A.G.M
APPRVD BY W.J.C.	AUGUST 1983

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CHAPTER 12

ROM

ASSEMBLY

Fit four 28 pin IC sockets to locations 10 - 13, then install sockets for IC's 9, 27, 28 and 29. After soldering, check all terminations for good connection, remove any excess solder flux or solder slivers.

Fit IC's 9 and 27 - 29 into their respective sockets. Insert the RA65 Monitor ROM into IC socket number 10. Note that if a 24 pin ROM is used as the RA65 monitor, ensure that pins 1, 2, 27 and 28 of the 28 pin socket are not used. That is, insert the RA65 monitor in the 24 pins of the socket closest to the keyboard. Failure to observe this, may result in destroying the ROM. Alternatively 24 pin sockets can be installed in socket locations 10 - 13. These should line up with the RAM sockets. The disadvantage of this type of socket is that it restricts the type of ROM's used to only 2732's. Thus expansion in the ROM area at a later time will be more difficult.

If the video display, RAM and CPU sections are completed the computer can be powered up and the video monitor should display the message " insert disk into drive A, press return ". This indicates that the system has powered up successfully. Refer to the software section of the manual for further details of the RA65 monitor.

CIRCUIT DESCRIPTION

The upper 32K of addressable memory in the Rabble 65 has been configured with page swapping to provide the user with the most flexible system of software selection on system initialisation. This feature provides the user with the ability to expand the available memory on board to over 100Kbytes, 48K of RAM and 56K of ROM.

The Rabble 65 permits the use of EPROMS, ranging from the 2732, 4K x 8 bit; 2764, 8K x 8 bit and the 27128, 16K x 8 bit. The page swapping drive configurations and mixing options are many. This manual will introduce the standard configuration and also the more natural expansion methods. Other combinations are possible, and this is left to users to derive their own requirements. All configurations permit RAM to operate in the range from $0000 - $7FFF.

The standard configuration

PAGE 0	RAM	$8000 - $BFFF	IC's 14 - 17 IC's 31 - 34	8 x 6116LP3	2K x 8 RAM

...

PAGE 1	ROM	$A000 - $BFFF	IC 13	1 x 2764	8K x 8 ROM
PAGE 2	ROM	$AOOO - $BFFF	IC 12	1 x 2764	8K x 8 ROM
PAGE 3	ROM	$AOOO - $BFFF	IC 11	1 x 2764	8K x 8 ROM
MONITOR	ROM	$E000 - $FFFF	IC 10	1 x 2764	8K x 8 ROM

Option 1

PAGE 0	RAM	$8000 - $BFFF	IC's 14 - 17 IC's 31 - 34	8 x 6116LP3	2K x 8 RAM
PAGE 1	ROM	$8000 - $BFFF	IC 13	1 x 27128	16K x 8 ROM
PAGE 2	ROM	$8000 - $BFFF	IC 12	1 x 27128	16K x 8 ROM
PAGE 3	ROM	$8000 - $BFFF	IC 11	1 x 27128	16K x 8 ROM
MONITOR	ROM	$E000 - $FFFF	IC 10	1 x 2764	8K x 8 ROM

Option 2

PAGE 0	RAM	$8000 - $9FFF	IC's 16 - 17 IC's 33 - 34	4 X 6116LP3	2K x 8 RAM
PAGE 1	ROM	$A000 - $AFFF	IC 13	1 x 2732	4K x 8 ROM
PAGE 2	ROM	$B000 - $BFFF	IC 12	1 x 2732	4K x 8 ROM
PAGE 3	ROM	$E000 - $EFFF	IC 11	1 x 2732	4K x 8 ROM
MONITOR	ROM	$F000 - $FFFF	IC 10	1 x 2732	4K x 8 ROM

Option 2 requires that the page swapping be disabled. This is most simply done by removing IC 27, the 74LS139.

ROM paging is controlled by the system VIA, IC 107, which is controlled by the system monitor. The start up routine is menu driven and assists the user to automatically select the correct ROM for the desired operating system.

The upper 32K block of memory is decoded into 4K blocks by a 74LS145, IC29. This is an open collector output, one of ten decoder. Address lines A12 - A15 are used to decode these blocks, of which the outputs are strap selectable to provide different configurations of paged ROM memory sizes. The selected outputs are low active, and are fed to OR gate inputs of IC 28, 74LS32. The outputs of these OR gates are connected to the CS pin of their respective ROM chips. The second input of the OR gates, are connected to one of the outputs of a two to four line decoder,

...

IC 27, 74LS139. The address line inputs of this chip are driven from the VIA to select one of four devices to be enabled.

1 RAM Page 0

2 ROM Page 1

3 ROM Page 2

4 ROM Page 3

The selected output provides a low level signal to the appropriate ROM page OR gate, IC 28, so that when the 74LS145, IC 29, outputs an address block (low signal) the output of the OR gate goes low, thus enabling the desired ROM.

Page 0, or the RAM page, is enabled by selecting page 0, or the system will automatically select this page when the disk system is selected. This signal is ANDed with the A13 address line, by IC 9, 74LS08. The output of this gate is ORed with A14 at IC 3, 74LS32, to drive the active low input of IC 2, 74LS138. IC's 2 and 3 are described in RAM stage 3.

The ROM sockets IC's 10 -13 are 28 pin devices. The pinouts of these 28 pin chips have been designed to complement the pin layout of the older 2716 and 2732 single supply ROM chips. When using 24 pin ROM chips, it is important to ensure that the chip uses the lower section of the socket, which, when correctly inserted, will line up physically with the 6116LP3 RAM chips.

The ROM chips are a memory device which contain non volatile memory cells. This memory is retained until the glass or quartz window is exposed to a light source with a wavelength of approximately 2537 Angstroms for a period of time. Programming of these devices is performed on an EPROM programmer, which stores the data on the data buss at the address selected on the address buss by the application of a high voltage pulse of several milliseconds. This then alters the bits in that location to those contained on the data buss. This condition is maintained almost indefinitely, or until the chip is erased.

The address and data lines of the ROM's are all in parallel, as with the RAM chips. The chips are selected as required by the address decoding and the resultant CS line is pulled low to activate the chip enable pin of that ROM. This permits the data at the selected address to be placed on the data buss and transported to the CPU.

The ROM chips have 12 - 14 address lines connected to them, depending on the size of ROM chip.

2732	4K ROM	12 address lines	A0 - A11
2764	8K ROM	13 address lines	A0 - A12
27128	16K ROM	14 address lines	A0 - A13

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6116LP3 2K RAM 11 address lines A0 - A10

DEBUGGING

This section of the computer contains three main areas, address decoding, page selection and ROM.

To check out the address decoding, test the outputs of the 74LS145, IC 29, pins 1 -7 and 9 to ensure the selected output pulses low, when the relevant address block is selected. Ensure that address lines A12 - A15 are reaching the decoder.

Paging can be checked out by testing the outputs of IC 27, 74LS139 to ensure that one output is low and the other three are high. Select each page and test again. If paging is faulty at this point, test the input signals which are supplied from the system VIA, IC 107, and if faulty refer to to the chapter describing the keyboard. Should the input signals be present, without switching the outputs, test that the enable input is at logic zero, otherwise the chip is faulty.

The page 0 output is connected to IC 9, 74LS08. Ensure that the strapping for this area is correct for the ROM configuration you have selected. The standard system will have a logic zero input to this gate with a resultant logic zero output. Address line A13 will have no effect on this output whilst page 0 is selected. IC 3, 74LS32, input is held low and A14 will control the input to enable IC 2, 74LS138 pin 4. Test this signal path through to IC 2, to clear the paging for RAM, page 0.

Pages 1, 2 and 3 when selected will send a logic zero signal to the appropriate gate at IC 28, 74LS32. Check that the signal reaches the gate and that when the address range of the associated ROM is selected, that the output of that gate pulses low. Any failure would indicate a faulty 74LS32 or incorrect strapping fo ROM size, adjacent to IC 29.

The monitor ROM chip select line is connected from IC 29, 74LS145 pin 11 via an invertor gate 74LS04, IC 47 and a four input NAND gate, 74LS20, IC 48. This is to provide for deselection of the RA65 monitor ROM when the following locations are accessed.

$F000 - $F003	decimal	61440 - 61443
$F400 - $F403	decimal	62464 - 62467
$F420 - $F423	decimal	62496 - 62499
$FC00 - $FC03	decimal	64512 - 64515

For a fault in this area, refer to the chapter on I/O Decoding.

The only other area to cause possible faults, is in the ROM's themselves. Check that no address lines, or data lines are shorted or

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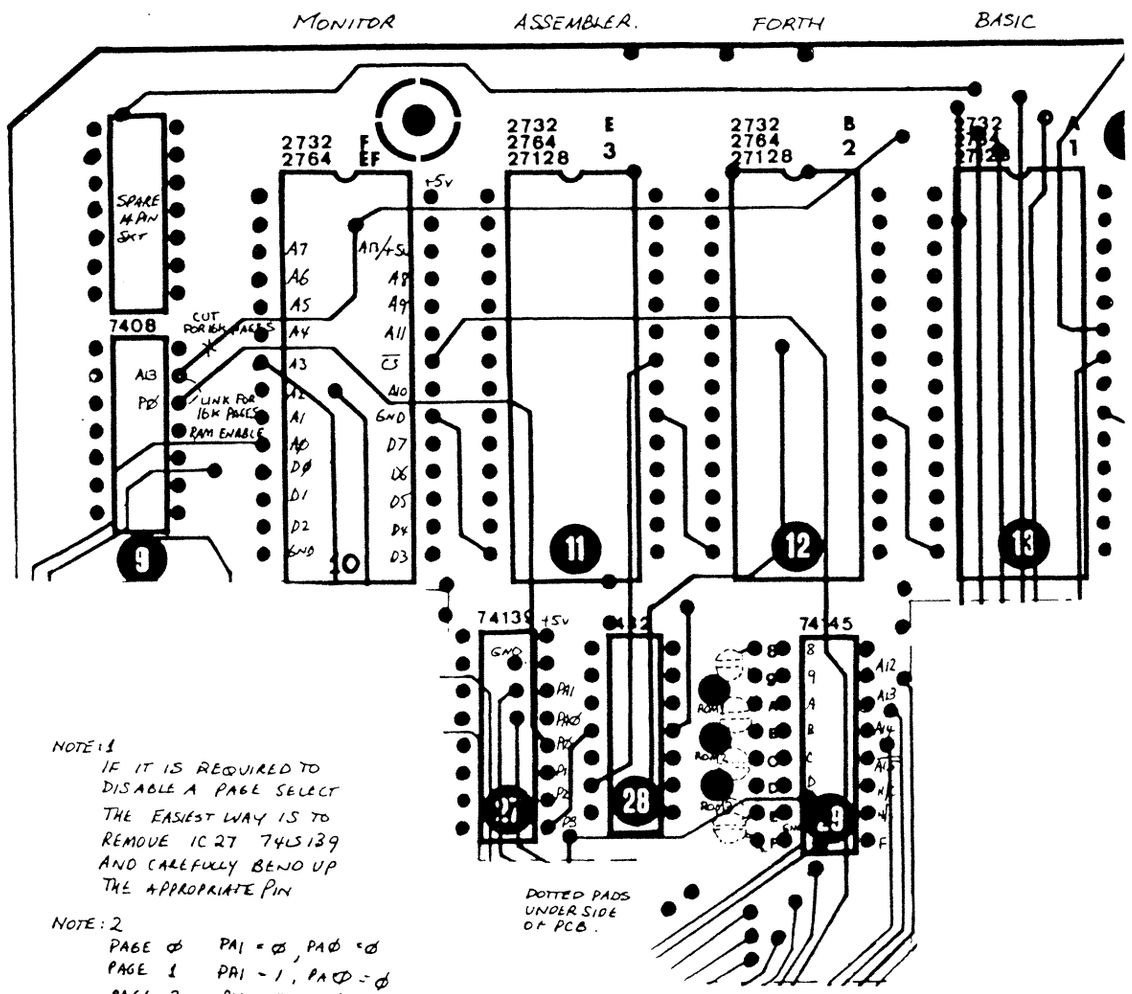
open circuit, and that the CS line is actually reaching the desired chip. If all is well, then the problem is contained within the ROM chip, which could be a failure of the chip , or a byte or block within the chip has been programmed incorrectly. Replace the chip with a known good chip to prove the fault.



NOTE: 1

IF IT IS REQUIRED TO DISABLE A PAGE SELECT THE EASIEST WAY IS TO REMOVE IC 27 74LS139 AND CAREFULLY BEND UP THE APPROPRIATE PIN

NOTE: 2

PAGE Ø	PA1 = Ø,	PAØ = Ø
PAGE 1	PA1 = 1,	PAØ = Ø
PAGE 2	PA1 = Ø	PAØ = 1
PAGE 3.	PA1 = 1,	PAØ = 1

NORMAL CONFIGURATION

8k BASIC 2764 ROM1
8k FORTH 2764 ROM2
8k ASSEM. 2764 ROM3.
8k MONITOR E, F.

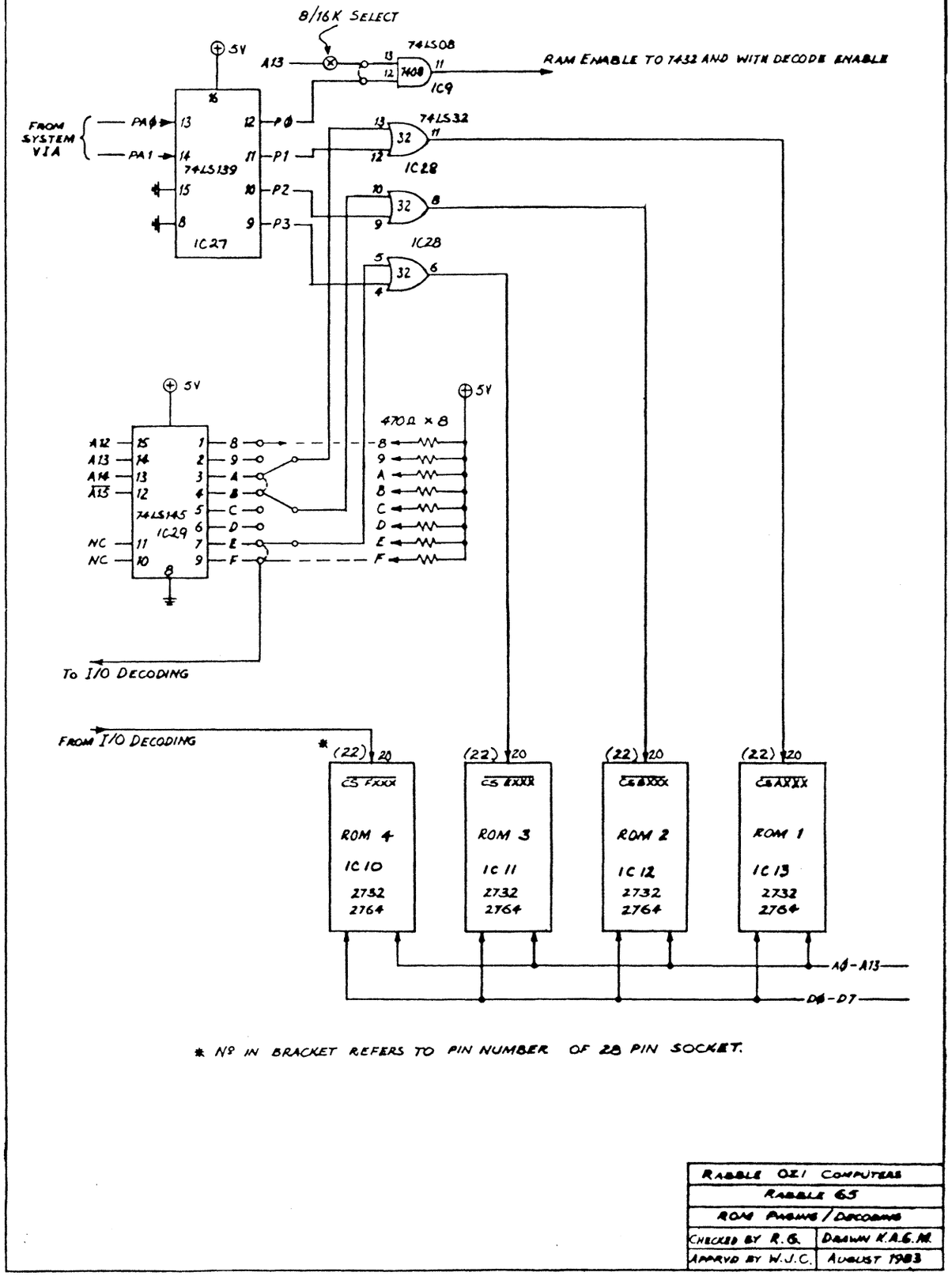
1. LINK PADS ON TOP OF PCB (3) TOGETHER.
2. LINK PADS ON UNDERSIDE OF PCB BETWEEN 'A' AND 'B'
3. LINK PADS ON UNDERSIDE OF PCB BETWEEN 'E' AND 'F'
4. CUT TRACK FROM 'E' TO ROM3 PAD.
5. CUT PAD TO '9' ON UNDERSIDE OF PCB.

EXTENDED CONFIGURATION

16K BASIC, 16 k FORTH, 16K ASSEMBLE/UTILITIES

1. MAKE MODS AS ABOVE BUT NOT Nos 5
2. LINK PADS BETWEEN '8' AND '9'
3. CUT PADS AT PIN 24 OF ROM1
   LINK PADS AT PIN 24 OF ROM 4
4. CUT TRACK TO PIN 13 OF IC9 7408
5. LINK PINS 12, 13 ON IC9 7408

NOTE: REGARDING 2764 EPROMS ON REVISION 1 AND 2 BOARDS PINS 27 AND PIN 1 SHOULD BE TIED TO +5V



* Nº IN BRACKET REFERS TO PIN NUMBER OF 28 PIN SOCKET.

RABBLE OZI COMPUTERS	
RABBLE 65	
ROM PINING / DECODING	
CHECKED BY R.G.	DRAWN K.A.G.M.
APPRVD BY W.J.C.	AUGUST 1983

CHAPTER 13

CPU

ASSEMBLY

Insert sockets for IC's 59 - 62, 74 - 77, 87 and 88. Fit resistor package, taking care of it's orientation, insert the two 390 ohm resistors, adjacent to IC 59, by standing them on their end. Fit the 16MHz crystal, other resistors, resistor pack and the reset switch. After all components are soldered into position, check all connections for dry joints or solder slivers. Clean off any excess resin deposits.

Insert chips into their respective sockets, taking care with the orientation of pin one of each chip. This completes the assembly of the CPU section.

CIRCUIT DESCRIPTION

This section of the Rabble 65 contains the CPU, address and data buffering, system clock generator and the NMHz switching.

The CPU is a 6502 chip, manufactured by a number of sources. It is not the aim of this manual to describe the internal architecture of the CPU or the methods of programming it. Many books are available from the larger bookshops on both the hardware and software relevant to the 6502.

The CPU operates when a clock signal is input to pin 37, IC 77, called phase 0 clock. This is the CPU's timing reference to select addresses on the address buss, and transfer the data to and from the data buss. A phase 2 clock signal is generated within the CPU chip, and this signal is output on pin 39. It is used to organise the timing of other chips on the Rabble 65, in particular the input / output ports and the address decoding.

The read / write (R/w) line is used to inform the memory and peripheral drivers which way the data will be transferred on the data buss. The data buss is bidirectional. A logic one on the R/w line indicates that the data will be read by the CPU, that is, data is transferred from memory or peripheral controller to a CPU register or accumulator. A low on the R/w line will output data from the CPU to be stored at the location pointed to by the address buss.

The reset line, when pulled low, halts the CPU and then when returned high will start the programme at the memory address pointed to by the data stored at address locations $FFFC - FFFD. The NMI and IRQ lines are tied high via pull up resistors to the +5V supply rail. These lines are not used on the Rabble 65, but appear on the expansion buss, with all the other lines neccessary for possible future expansion.

The system clock is derived from a 16MHz oscillator, made up of IC 59, 74LS04, a 16 MHz crystal and two 390 ohm resistors. The output of the oscillator is buffered by another gate of IC 59 to minimise the loading of the oscillator circuit.

The 16MHz signal is used to drive the video dot clock and is also divided down to provide other clock rates for the CPU, serial I/O and floppy disc controller timing. The divider used is a 74LS393, IC74, which is a dual 4 bit binary ripple counter. These two sections are connected in cascade to provide, from the 16MHz input signal, outputs of 8, 4, 2 and 1MHz, and 500, 250, 125 and 62.5KHz.

The 125 and 250KHz signals are made available for the floppy disk controller's data timing. The 4MHz signal is used for the serial I/O baud rate generator reference, as well as for the CPU clock generator.

The 4MHz signal, used for the CPU phase 0 clock, is divided by two or four by the 74LS76, IC 76, dual J-K flip flop. The division factor is determined by the chip select line CSC000 - C7FF. The Rabble 65 can select a system of clock speed switching to enable an increase of execution speed of nearly 100%. This system is called NMHz switching. The lower 48K and the upper 14K of the address range, always accesses RAM or ROM, is capable of operating with a system clock in excess of 2MHz. The other 2K of the address range, $C000 - $C7FF, accesses a number of I/O devices interfacing to human operators and low speed devices. Some of the interface chips cannot operate at the higher speed and even if they could the operator can only operate at a fraction of this speed. Therefore, to double the system operating speed, the system clock runs at 2MHz for all addresses other than that in the $C000 - $C7FF range which runs at 1MHz.

When the $C000 - $C7FF range of memory address range is accessed, CS line $C000 - $C7FF goes low, this signal is fed to one of the inputs of IC 75, 74LS30, an eight input NAND gate. This normally high input, together with all the other inputs being tied high, provides a low output signal to IC 76, 74LS76, inputs. Whilst this input is low, this stage of the flip flop has it's output set and provides a logic one output to the second half of the flip flop, which always divides by two, providing, in this case, a phase 0 clock frequency of 2MHz.

For addresses in the $C000 - $C7FF range the output from IC 75 goes high. Flip flop IC 76, is set in the toggle mode and the clock inputs to pin 1 are divided by 2, thus enabling the second half of the flip flop for only one clock period in two. The second stage of IC 76 also divides by 2, to provide an output signal of 1MHz for the phase 0 clock.

The standard Rabble 65 is set for 1MHz operation for all addresses, during production. To enable the NMHz switching, cut the link on the bottom of the board from pin 6 of IC 75 to ground. The system clock can also be doubled again, by selecting the 8MHz output from IC 74, 74LS393, in lieu of the 4MHz output. Strapping for this can be performed on the underside of the PCB. Memory chips to operate at this speed are not generally available at the time of writing.

The last area of the CPU section is the address and data buffers.

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These lines, and also the phase 2 clock and the R/w line are all buffered immediately after the CPU to minimise buss capacitance and device loading from affecting the CPU. Another use of the buffers is to provide external control for the Rabble 65. Which will permit another processor to deactivate the CPU and have direct memory access to the Rabble 65.

The sixteen address, phase 2 clock and the R/w lines are connected to three 74LS367's, hex three state buffers, IC's 60 - 62. These buffers operate in one direction only, away from the CPU, and are always held activated in the standard Rabble 65. The data lines are connected to a 74LS245, IC 87, a three state octal transceiver. This chip is a bi-directional device controlled by the inverted R/w line. The R/w line is inverted by IC 88, 74LS04.

The data and address line buffers are held enabled by a low signal on their enable inputs. This line is commoned to all four chips and extended to the expansion connector. To enable control to the expansion connector, this ground line must be disconnected by cutting the track on the bottom of the PCB, just below the connector.

The microprocessor used in the Rabble 65 is from the 6502 family. Later versions may contain the Rockwell 65C02. this latter chip is a CMOS version of the 6502 and contains some new instructions and two new addressing modes. It is also capable of running at higher speeds and requires less power to operate at normal speeds.

CHIP	6502	65C02
Manufacturer	Rockwell MOS Technology Synertek	Rockwell
No. Instructions	56	68
Addressing Modes	13	15
Accumulator	1 - A	1 - A
Index Registers	2 - X,Y	2 - X,Y
Other Registers	Stack Pointer Processor Status	Stack Pointer Processor Status
Stack	256 Bytes	256 Bytes
Status Flags	NCVIDB	NCVIDB
Interupts	IRQ, NMI	IRQ, NMI
Resets	1	1
Addressing Range	64K	64K

Address buss	16 Bit	16 Bit
Data Buss	8 Bit	8 Bit
Supply Voltage	+5V	+5V
Power Dissipation	0.25 Watt	0.05 Watt
Clock Frequency	1MHz	1MHz

1MHz is the standard clock rate catered for, however, if the support chips are upgraded to operate at higher frequencies, then the clock rate can be increased to 2MHz.

A0 - A15. The address buss, pins 9 - 20 and 22 - 25.
The address on this buss changes and becomes valid during a phase 0 clock cycle and remains valid through the phase 2 clock cycle. The address buss only carries addresses away from the CPU to the rest of the computer.

D0 - D7. The data buss. Pins 26 - 33.
This buss is bidirectional, where data is read from the buss by the CPU or data is written to the buss by the CPU, depending on the state of the R/w line. To read data from the buss, the data must be stable 100nS before the falling edge of the phase 2 clock for the CPU to accept it. The CPU must have steady data on the data buss 300nS prior to the falling edge of the phase 2 clock, and the data must remain steady for another 50nS for it to be accepted by the memory or peripheral system.

R/w. The read / write line. Pin 34.
This line becomes valid at the same time as the address buss, and goes high for a read cycle and low for a write cycle.

Phase 0 Clock Pin 37.
The phase 0 clock is the clock signal supplied from the crystal oscillator and divider which is fed into the CPU. The phase 2 clock is derived from this clock.

Phase 1 Clock. Pin 3 This line is not used.

Phase 2 Clock. Pin 39
The phase 2 clock is the line which controls the timing of memory and peripherals of the computer. All timing throughout the system including that of the CPU is referenced to this clock.

RDY Pin 2. The ready input to the CPU.
Pulling this line low during the phase 1 clock cycle will halt the CPU. The address buss will hold the address of the current location being fetched.

NMI and IRQ Pins 6 and 4.
Non Maskable Interupt and Interupt Request lines. When these lines are pulled low, the CPU ceases operation on the current instruction and the programme restarts at the vectors stored at addresses in ROM locations $FFFA - FFFB and $FFFE - FFFF, low byte - high byte, respectively. The IRQ can be ignored if the interrupt flag is set in the CPU.

RES pin 40. Reset.
This line is normally held high except when resetting is required. When reset, the CPU starts the programme at the address stored in ROM at locations $FFFC - FFFD.

S.O. Pin 40. Set Overflow. Not used

SYNC Pin 7 Not used

N.C. Pins 5, 35 and 36. These pins are not connected.

DEBUGGING

To enable debugging of this section, it is assumed that a known good monitor ROM is in IC 10 position, and that a known good RAM chip is in IC socket 25.

Test the 16MHz oscillator at the input to the divider chip IC 74, pin 13. Check that 4MHz is present at pin 10 and that 125KHz is present at pin 5 of IC 74. If all is well, then check that 4MHz is present at pins 1 and 6 of IC 76. The output of this latter divider is pin 11, which should have a 1MHz signal for the standard system. If NMHz switching is enabled, then the output will be 2MHz.

Test address line buffers, IC's 60 - 62, by ensuring that supply rails are normal, and that pins 1 and 15 of each chip are tied low. Check address line A0 at the input of the buffer, IC 62 pin 2, and ensure that a similar signal appears on it's output, pin 3. A logic probe is ideal to test this area with. The pulse lamp should glow to indicate changes in logic levels at both input and output of the buffers. Follow through each buffer stage of these three IC's, include the phase 2 clock and the R/w line.

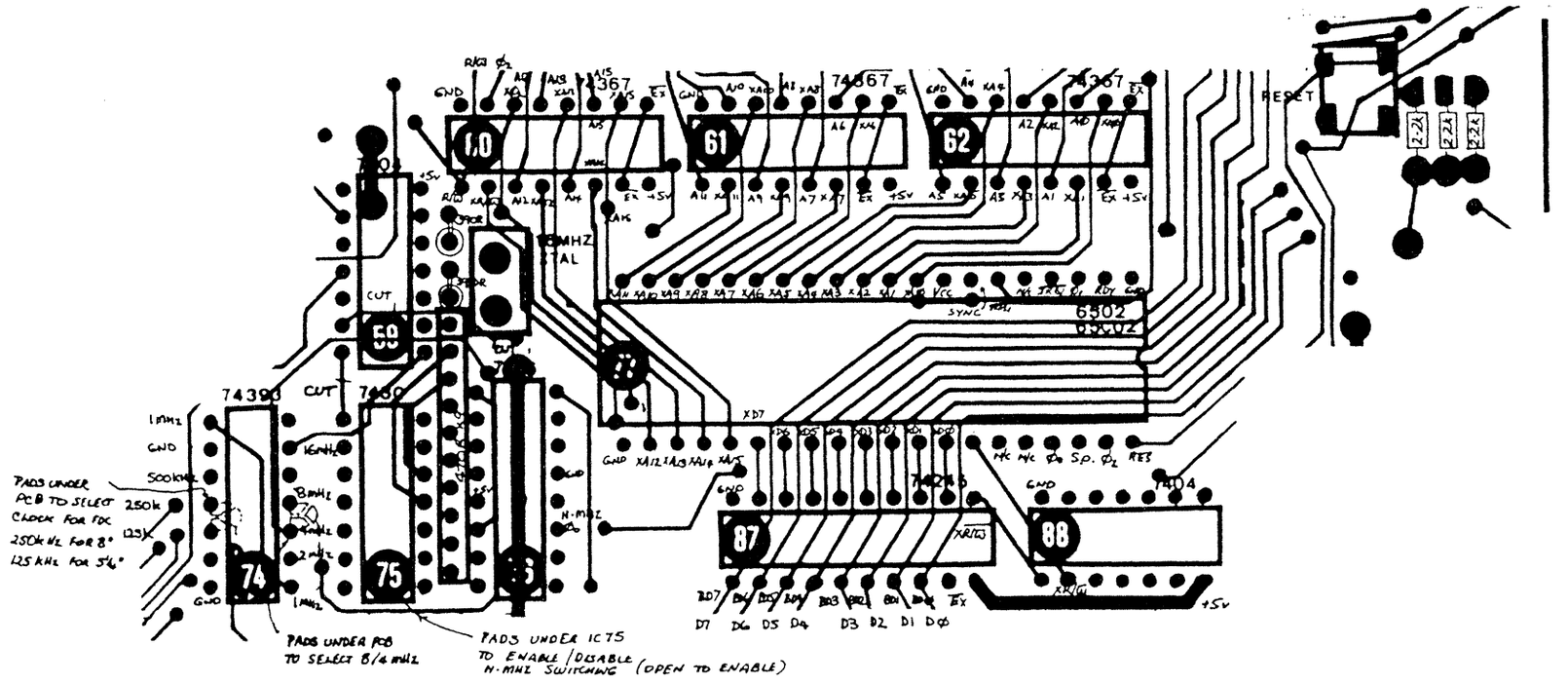
Test the data transceiver, IC 87 74LS245, by ensuring that pin 19, the enable pin is low, and that data is being passed through the data

transceiver in the correct direction. It may be easier to determine correct operation, by removing IC's 77 and 88 (remove power first). Tie pin 1 of IC 87 low, then feed a logic pulse train to pin 2 of IC 87, it should appear on pin 18. A signal applied to pin 18 should not appear on pin 2, until pin 1 is raised to logic one. Check the remaining inputs for correct operation. Replace the removed chips.

The R/w line from pin 34 of IC 77, 6502, is inverted by IC 88, 74LS04, check pin 9 for the R/w signal and ensure that the inverted signal is at pin 8 and that it reaches the data transceiver at pin 1.

The only other chip in this section is the CPU chip. Ensure that the supply rails are connected to the chip. Pins 1 and 21 are ground and pin 8 is +5V. Check that the RES, IRQ and NMI, pins 40, 4 and 6 are all tied to rail volts via 1Kohm resistors. See that pin 40 goes low when the reset button is depressed.

If the CPU is still suspected as being faulty, and the problem is not related to any other section of the board, then try replacing the CPU to clear it of any suspicion.

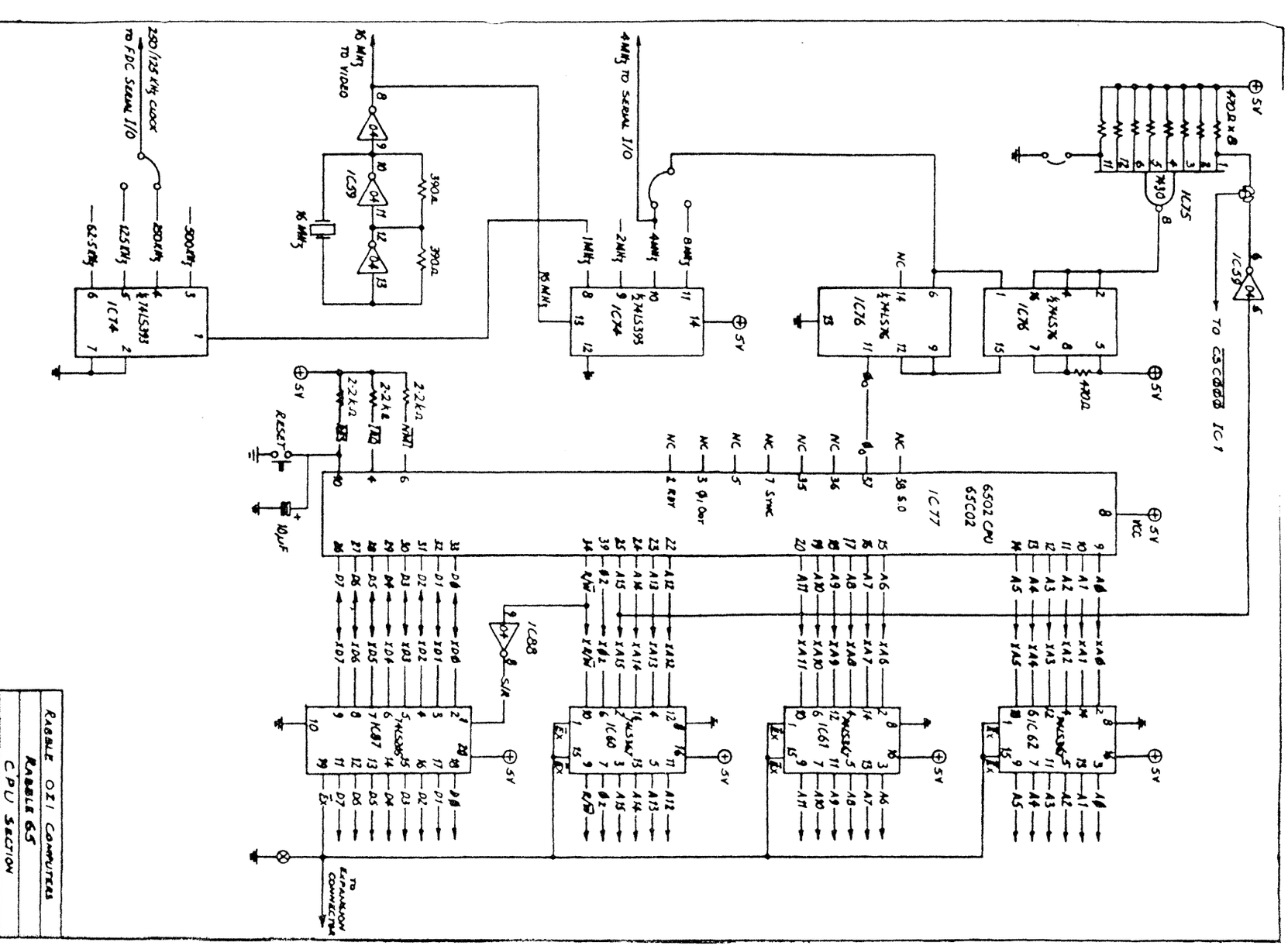


NOTES: ON THE N-MHz SWITCHING.

STANDARD BOARDS HAVE THE N-MHz SWITCHING DISABLED TO ENABLE, CUT THE LINK BETWEEN PADS UNDER IC75

THIS ALLOWS C3C000 TO CONTROL THE CPU ϕ_0 CLOCK

ALL PROGRAMS OUTSIDE THIS ADDRESS BLOCK WILL RUN AT 2 MHz, C000-C7FF WILL RUN AT 1MHz



RABBLE 65		
CPU SECTION		
CHECKED BY R.G.	DRAWN K.A.G.M.	
APPROVED BY W.J.C.	AUGUST 1983	

RABBLE O.Z.I. COMPUTERS

CHAPTER 14

I / O DECODING

ASSEMBLY

IC's 47 - 52 and 65 - 68 provide the major decoding for the system peripherals, including the video display and the keyboard. Thus all sockets should be populated in this section to operate even a minimum system configuration.

All IC sockets should be installed, taking care to orientate them correctly. The pin 1 end of the socket should appear at the top left of each IC socket location. Solder all pins of each socket, checking each joint carefullyto ensure no solder blobs or splashes exist. If neccessary clean excess flux away with a cloth dampened with methylated spirits.

Insert each chip as indicated on the component layout, to complete the assembly.

CIRCUIT DESCRIPTION

The I/O decoding provides decoding for two distinct areas of the memory map. The first is in the $C))) - $C7FF, decimal 49152 - 51199 block, the other is in the $F000 - $FFFF, decimal 61440 - 65535, block. This latter block is shared discretely with the monitor ROM.

The $C000 - $C7FF block decoding is enabled by the CS$C000 line from the RAM 3 decoder chip, IC 1. This line is used to enable IC 66, 74LS138, where address lines A8 - A10 decode eight blocks of 256 bytes. The blocks $C000 - $C0FF, $C400 - $C4FF and $C700 - $C7FF are the only outputs used, and appear on pins 15, 11 and 7 respectively.

$C000 - $C0FF, or to simplify $C0xx, output from IC 66 is fed to the enable gate of IC 67, yet another 74LS138, where address lines A4 - A6 are used to break this 256 byte block down to 16 byte blocks. The A7 line is used to enable this chip so that no images are produced in the memory map. Thus we end up with only eight 16 byte blocks, totalling 128 bytes. Outputs from pins 15, 14 and 9 of IC 67 are the only ones used on the Rabble 65. These outputs are used to further decode areas of memory within the $C00x and $C01x blocks, and the third output is used to select the system VIA at address locations $C06x.

Each of the blocks $C00x and $C01x are further divided down to provide 4 byte blocks, IC 68, a 74LS139. Address lines a@ and A3 are used with the relevant 16 byte line to decode each of the four 4 byte blocks. The The final decoded blocks are $C000 - $C003 which is the address location of the floppy disk controller's PIA, to control the parallel section of the disk drive. The next block used is $C010 - $C013, the address location of the floppy disk controller's ACIA, which transfers serial data to and from the disk drive. For further details on the FDC,

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you are referred to chapter 9.

The third block used from the 74LS139, IC 68, is to enable the 6845 CRTC, IC 57. This enables the system to access the registers of the CRTC to read or alter values of these registers. For more information on the CRTC, refer to chapter 6.

The system VIA uses the $C06x range, decimal 51056 - 51071, and is used to initialise a number of areas on the Rabble 65 including the ROM paging, baud rate generator and is also used to assist with the reading of the keyboard.

From IC 66, 74LS138, two other outputs are used. $C4xx and $C7xx. The $c4xx block, decimal 50176 - 50431, is used to select the keyboard RIOT chip, IC 108 - 6532. The function of this chip is discussed in chapter 5. The $C7xx output is further decoded by IC 46, 74LS138. Address lines A4 - A6 are used to decode eight 16 byte blocks. Address line A7 enables the chip whilst that input is low, hence only the lower half of the $C7xx block is decoded, and no images are produced.

The eirht outputs from IC 46, 74LS138, are 16 byte blocks from $C70x through to $C77x. The first four of these are used to drive 16/18 pin I/O buss. These outputs are discussed in more detail in chapter 10.

The second major section of the I/O decoding is used to decode four small blocks of memory in the $Fxxx block. This block is primarily used for the system monitor, and it has areas reserved within it to provide for a serial and a parallel port. These locations are each four bytes wide and the start addresses of each block is:-

$F000	decimal	61440	Serial I/O
$F400	decimal	62464	Parallel I/O
$F420	decimal	62496	Printer Strobe
$FC00	decimal	64512	Serial I/O

IC's 50, 74LS138; 48, 74LS20 and 52, 74LS27 are used to decode the primary areas of $F000 - $F003, $F400 -$F403 and $FC00 - $FC03, with images $20 bytes higher. IC 48 is used to enable one of the enable gates of the 74LS138, IC50. IC 48, is a four input NAND gate, which has address lines A12 - A14 and inverted A15 as inputs. Thus when all of these address lines are high, block $Fxxx selected, the output will be low to enable one input of IC 50, 74LS138.

The next enable input of the 74LS138, IC 50, is controlled by half of IC 52, 74LS27 - three input NOR gate, which has the address lines A6 - A8 as its inputs. To enable the logic 1 input of the 74LS138, these address lines to IC 52 must all be at logic 0.

The third enable input of the 74LS138, IC 50, is enabled with the aid of the other half of IC 52, 74LS27, and an inverter gate of IC 51,

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74LS04. Address lines A2 - A4 are required to be low to provide a logic one to the inverter, which in turn enables the input of IC 50, 74LS138, with a logic zero.

This leaves address lines A0, A1, A5, A9 - A11 undecoded. A0 and A1 do not require decoding, as a four byte block is required. Address lines A9 - A11 are decoded using the binary inputs of the one of eight decoder, IC 50. The outputs of the 74LS138 thus provide outputs of:-

$F000
$F200
$F400
$F600
$F800
$FA00
$FC00
$FE00

Each of these decoded addresses is four bytes wide and because address line A5 has not been used for decoding, images will occur in each of these blocks $20 bytes higher.

The blocks $F000 and $FC00 are required to enable the serial I/O and must be brought together as a single signal. IC 52, half 74LS27, is used for this purpose. Pins 9, $FC00, and 15, $F000 (with images) are fed into two of the inputs of one 74LS00 NAND gate with the output inverted, to provide an AND gate, such that when either the $F000 or $FC00 line is selected from IC 50 the input to IC 52, 74LS27, goes low.

With address line A5 low the output of IC 52, 74LS27, becomes high. This signal is inverted by IC 51, 74LS04, to provide the select line for address locations $F000 - $F003 and $FC00 - $FC03. At the same time this signal is used to inhibit access to the monitor ROM by placing one of the inputs of IC 48, 74LS20 - a four input NAND gate, at a logic zero. This provides a logic one output, thus deselecting the monitor ROM. Other inputs to IC 48 are from the line printer strobe enable, the line printer select line and also the CS line for the monitor ROM. This disables the monitor ROM when either the RS232 or the Centronics ports are accessed, or when the monitor ROM is not required by the system.

Output 2 from the 74LS138, IC 50,provides the information for both $F400 - $F403 and $F420 - $F423. These blocks must be separated to control the Centronics port. To decode the $F400 line, address line A5 is inverted and the resultant signal is NANDed with the inverted output from IC 50, pin 13. Thus the line printer is selected only when address block $F400 - $F403 appears on the system address buss. This select line is also used to inhibit the monitor ROM at IC 48, 74LS20, as described earlier. The inverted $F400 / $F420 line from IC 50, is fed to another NAND gate, IC 49, 74LS00, and is NANDed with the A5 address line to provide a low output when A5 is high. This enables the line printer strobe pulse generator, and at the same time disables the monitor ROM, via IC 48.

DEBUGGING

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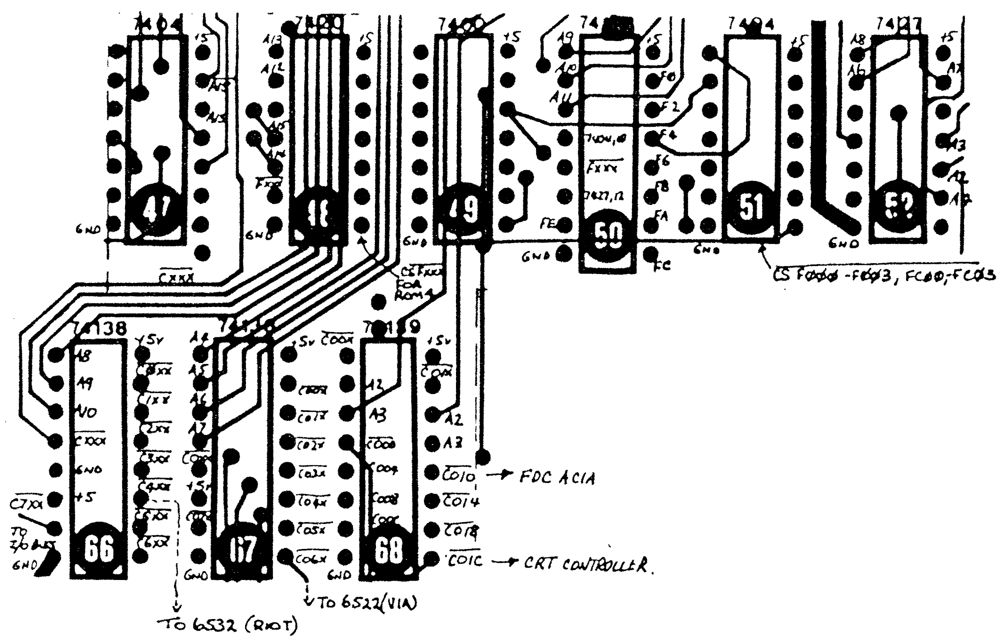
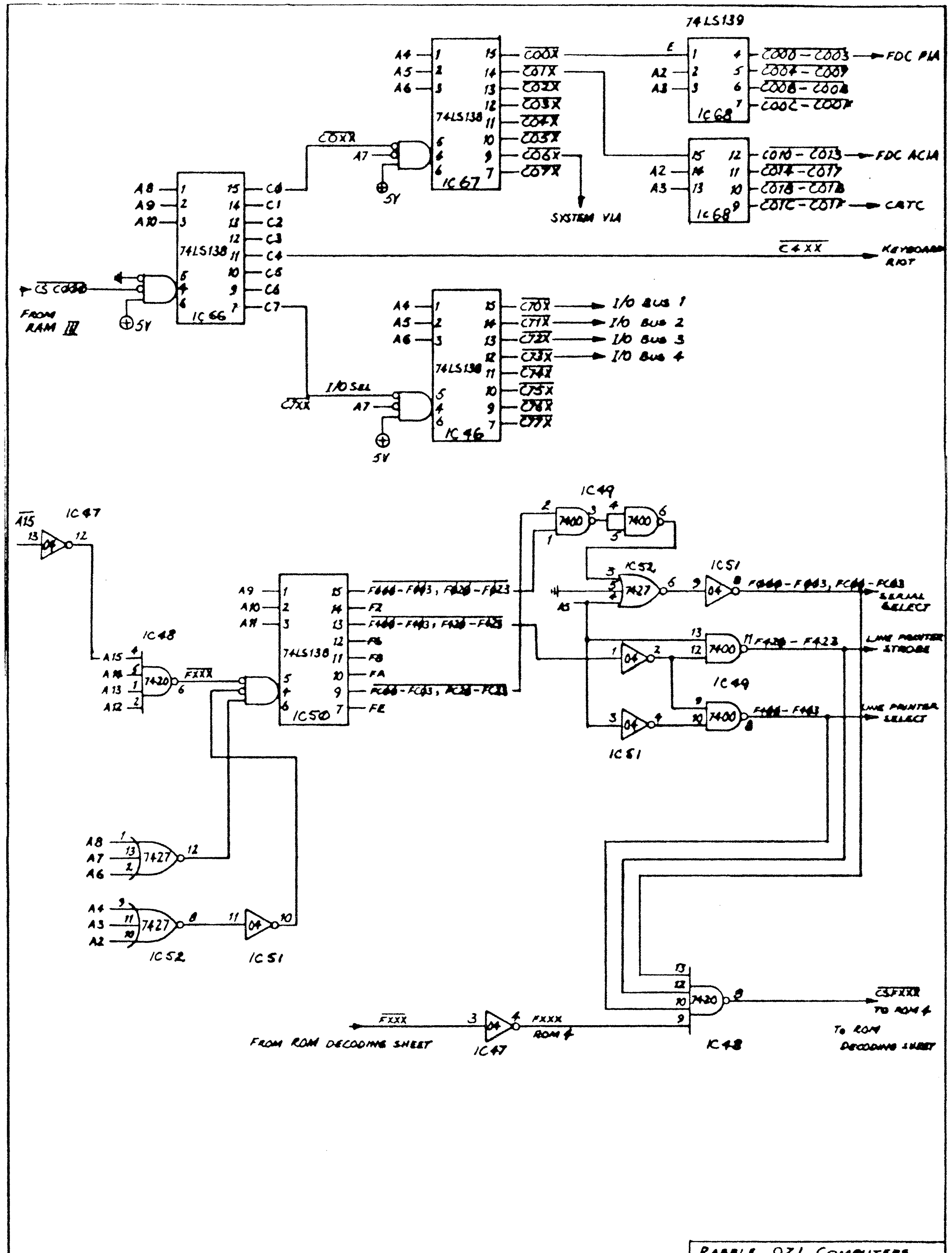
There are two ways to locate faulty areas in this section of the computer. The first is to note which areas of the decoding are effective, and eliminate the working areas, to leave you with the common component which controls all of the areas which do not work. The second method is to follow the system decoding, testing each point with a logic probe whilst performing a CPU read from that location.

For address locations in the $Cxxx block, ensure that a low going pulse is coming from pin 15 of IC 1, 74LS138, and that it reaches pin 5 of IC 66, 74LS138. The next point to test for low going pulses is the output of IC 66 at pin 15, which should reach pin 4 of IC 67, 74LS138. This chip should output pulses on pins 14 and 15, when access to $C00x or $C01x is performed. These pulses should then appear on pins 1 and 15 of IC 68 respectively. Output pulses should appear on pins 4 and 12 of this IC when access is made to $C000 and $C010. Ifthe pulses should fail to appear , then the fault lies between the last successful test point and the first point at which the signal disappeared. Check for the keyboard signal at pin 11 of IC 66, 74LS138, and the 16/18 pin I/O buss at pin 7 of IC 66.

For decoding locations in the $Fxxx range, set the computer up in the monitor ROM by pressing the reset key, to ensure that the $Fxxx region is selected. Test pin 9 of IC 29, 74LS145, for low going pulses. They should be there if the video display, is displaying it's start up menu. This pulse will also appear on IC 48 input, and output to the monitor ROM chip select. The other output from IC 48, 74LS20, should also be outputting the same signal at this stage, pins 6 and 8 of IC 48. Ensure that IC 52 is functioning by testing pins 5 and 6 of IC 50, 74LS138, for pulses, indicating that address lines A2 - A4 and A6 - A8 are present. Test pins 1, 2 and 3 of IC 50, for the presence of address lines A9 - A11. Using the monitor, read from, or write to addresses being decoded by IC 50, eg $F000, and test the relevant output for a low going pulse, (it is most probable that a number of locations will show a number of these pulses). Test the inputs to IC 52, 74LS27 to ensure that the ANDed signals from IC 50 and address line A5 are present, and also that the output is present as a high going pulse. Check IC 47, 74LS04, to ensure this signal is inverted and reaches the appropriate input of IC 48, 74LS20. Ensure that when an input to IC 48 goes low, that the output goes high. Check that the signal from pin 13 of IC 50, 74LS138 is inverted and correctly NANDed by IC 49, 74LS00.





RABBLE OZI COMPUTERS	
RABBLE 65	
I/O DECODING	
CHECKED BY R.G.	DRAWN K.A.G.M.
APPRVD BY W.J.C.	AUGUST 1983

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CHAPTER 15

GLOSSARY

6502
The manufacturer's name for the CPU within your Rabble 65.

ACIA
Asynchronous Communications Interface Adapter. This chip provides the means of converting data from a serial format to parallel and parallel to serial.

Address
(N) The number associated with each memory location. The address range on your Rabble 65 is $0000 - $FFFF (decimal 0 - 65535). (V) To refer to a particular memory location.

Address Buss
The set of wires, which carry the binary encoded address from the CPU to the rest of the computer.

Addressing Mode
The 6502 CPU has thirteen different methods of referencing memory locations. The 65C02 has fifteen different methods. These various methods are referred to as addressing modes.

Analogue
Analogue measurements, as opposed to digital measurements, use an infinitely variable quantity to represent values. Digital measurements use precise, stepped quantities in finite increments to represent values.

AND
A binary function which is logic one if and only if all it's inputs are logic one.

ASCII
Acronym for American Standard Code for Information Interchange. This is a standard code which assigns a unique value from $00 - $7F (decimal 0 - 127), to each letter, number or control character used in the Rabble 65.

Assembler
A programme which converts the mnemonics of assembly language into the opcodes and operands of machine language.

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Assembly language
A high level language similar in structure to macchine language, but operates with mnemonics and symbols. Programmes are easier to write and understand in assembly language than in machine code.

BASIC
Acronym for Beginner's All-purpose Symbolic Instruction Code. This is a high level language invented in 1963. It is possibly the most widely used language in home computers.

Baud
This is the term given to describe the rate at which data is transferred along a wire.

Binary
A number system based on the numbers 1 and 0. Each digit represents a power of two. The advantage of binary is that it is easy to represent a binary number on a wire, simply by the presence or absence of a voltage on that wire.

Binary function
An operation performed by an electronic circuit which has one or more inputs and one output. The functions most often encountered are AND, OR, NOT and E-OR.

Bit
The smallest amount of information which a computer can handle. A single bit can have a value of 0 or 1. Bits can be grouped to form larger values to produce a nibble or byte.

Board
Printed circuit board.

Boot
To get the system up and running from a cold start, usually referred to disk systems.

Buffer
(1) A device used to isolate one circuit from the loading effects of another. (2) An area of memory which is used to hold data tempoarily.

Bug
An error. Bugs can be either hardware or software orientated. A hardware bug relates to an electronic or physical component. A software bug refers to a programming error.

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Burn
To burn an EPROM, is to store a programme in an EPROM using an EPROM programmer.

Buss
A group of wires in a computer which carry a related set of data from one point to another.

Byte
A basic unit of computer memory. A byte is made up of eight bits.

Character
Any graphic symbol which has a specific meaning. These include all alpha numerics as well as ASCII control codes and games symbols stored in the character generator.

Chip
Integrated Circuit.

Circuit diagram
A diagram which represents the electronic components and their interconnections of an electronic apparatus.

Code
A method of representing data using other terms. The ASCII code represents characters as binary numbers, the BASIC language represents algorithms in terms of programme statements. Code is also used to refer to programmes, usually written in low level languages such as machine code.

Cold start
To begin to operate a computer from the reset condition or from power on.

Computer
An apparatus which can act on a set of instructions in a predictable fashion. These instructions and data can be changed as required.

Control character
Characters in the ASCII character set which usually have no graphic representation, but are used to control various functions. For example, the RETURN control character is a signal to the Rabble 65 monitor that you have finished inputting a line, and that you are ready for the CPU to act upon it.

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CPU
See microprocessor

CRT
Cathode Ray Tube, a television screen or an apparatus containing a television screen.

CRTC
A CRT Controller. This device is software controlled and looks after the regimen of the CRT updating.

Cursor
A symbol which indicates where the next character is going to be typed on the screen.

Data
Information. Singular datum.

Debug
To locate a bug and rectify it.

Digital
The term given to a device which makes calculations in binary format. These digits are either a logic one for a true value or logic zero for a false value or statement.

DIP
Dual In line Package, the standard container for all IC's used on the Rabble 65.

Disassembler
A programme which converts the opcodes of machine language to the mnemonics of assembly language.

Disk
A circular sheet of mylar, coated with a ferrous substance. These disks are usually enclosed in a protective sheath with holes to enable access to the recording medium. The disk stores data in a non volatile format for later reuse by the computer.

Disk Drive
The hardware used to rotate the disk and to transfer the data to and from the disk under control of the computer.

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Display
An output device from the computer which indicates information to the operator, usually a CRT.

Entry point
The location used by programmes, which contains the first executable instruction. Usually referred to in machine code subroutines.

EPROM
Eraseable Programmable Read Only Memory. An EPROM is a ROM whose contents can be altered by electrical means. Data in EPROMs is retained when power is turned off. The EPROMs used in the Rabble 65 can be erased by exposing them to ultraviolet light and can then be reprogrammed.

Execute
To perform a command or instruction, or to run a group of these, called a programme.

Format
The physical form in which something appears.

Graphic
A character which has a pictorial representation rather than an alpha numeric representation.

Hardware
The physical components of a computer.

Hexadecimal
Hex or $, a number system based on the number 16. The number system uses digits 0 - 9 and letters A - F to represent in a single unit the numbers 0 - 16. Each hex digit represents a power of 16. This manual refers to all hexadecimal numbers by prefixing them with the ($) sign, eg $C7FF.

High level language
A language which is more intelligble to humans than to the computer. The computer then translates this to a language it can understand.

High byte
The high order byte of a two byte address. In the 6502 series of CPU, the high byte of the address is stored after the low byte in consecutive memory locations.

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Hertz
Hz. Frequency in cycles per second. The reference oscillator runs at 16,000,000Hz, or 16MHz.

I/O
Input / Output.

IC
Integrated Circuit.

Input
A data stream going into the computer from it's peripherals. To obtain data from the outside world.

Input / Output
The software or hardware which exchanges data with the outside world.

Instruction
The smallest portion of a programme that a computer can excecute. The machine language code in the Rabble 65 is made up of one two or three byte instructions. High level languages can use instructions many characters long.

Integrated circuit
A small wafer of silicon material, into which has been etched an electronic circuit. A single IC can contain thousands of discrete electronic components. They are usually housed in DIP's.

Interface
An electronic device which makes possible the interchange of information from one device to another.

Interpreter
A programme which understands and excecutes a high level language. BASIC programmes are handled by a BASIC interpreter.

Interupt
A signal which indicates to the computer that a routine is required to be performed urgently. When the CPU receives such a signal, it finishes the instruction it is performing and then services the interupt, after which the CPU is returned to that point of the programme where the interupt took place.

K
Normally means thousand, hence 1KHz is equal to 1000Hz. When

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referenced to memory, K represents 2 to the tenth power or 1024.

Keyboard
The means of most communication from the operator to the computer. The keyboard converts the pressed key to a voltage which the computer calculates and then gives a value to it for the CPU to recognise.

Kilobyte
1024 bytes, or $400 bytes.

Language
A computer language is a code which the computer and programmer communicate with. The programmer dictates what he wants done, and the computer decodes the code and performs the instructions.

Line
(1) On a CRT, a line is a horizontal line of pulses displaying part of a graphic display from the left of the screen to the right side. (2) An input line is a string of characters input from the keyboard to the computer.

Low byte
The low order byte of a two byte address. In the 6502 series of CPU the low byte of the address is stored in the first byte of a pair in successive memory locations.

Machine language
The lowest level language which a computer understands. Machine languages are usually binary, although most machines operate with Hex. Instructions in machine language are single byte opcodes, followed by a one or two byte operand if required.

Memory address
A memory address is a two byte Hex value which selects a single memory location out of the memory map.

Memory location
The smallest subdivision of the memory map to which the CPU can refer. Each memory cell and I/O device has a unique address. Each location of memory can hold one byte of data.

Memory map
This is a pictorial display of the system's memory allocation.

Microcomputer

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A computer which is designed with a microprocessor as the CPU.

Microprocessor
An integrated circuit which understands and excecutes machine language programmes, sometimes referred to as a CPU, central processing unit.

Mnemonic
A symbol or group of symbols used to assist the operator to remember the code. In assembly language, each instruction is given a three letter mnemonic to represent an eight bit binary value.

Mode
A condition or set of conditions under which a certain set of rules apply.

Monitor
(1) A CRT display. (2) A programme which permits you to use the computer at a low language level.

Multiplexer
An electronic circuit which has more than one data inputs, selector inputs, and only one output. The device connects one of the inputs to the output, determined by the code on the selector inputs.

Nibble
Half a byte, or four bits.

Opcode
A machine language instruction, usually a numerical value given in hex.

OR
A logic gate whose output is logic one if any of it's inputs are at logic one.

Output
Data generated by the computer which is to be delivered to the outside world.

PIA
Peripheral Interface Adapter. This is an IC which can transfer, under computer control, data to and from the outside world. The PIA is also used to control the Rabble 65's floppy disk drives and the parallel printer port.

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Page
(1) A block of memory, containing 256 consecutive locations. In the Rabble 65 a page starts with the low byte address value at $00 and ends when it is $FF. (2) When referenced to the ROM paging a page is that area of memory which is switched in or out of circuit as required, in the standard Rabble 65 this block is 4Kbytes.

Pascal
A high level language.

Peripheral
A piece of hardware attached to the computer which is not a part of the computer itself. Peripherals are generally some sort of I/O device.

Port
A group of I/O lines controlled by the PIA or other I/O device. Usually in groups of eight bits.

Printed Circuit Board (PCB)
The substrate on which your computer is built upon. It is a fibreglass sheet with a layer of copper glued to each side. Areas of the copper have been removed to leave a set of tracks to connect components on the board to each other. These components are then soldered onto the board, to provide the completed assembly.

Programme
A sequence of instructions which dictate the flow of operation to the CPU.

PROM
See EPROM.

Random Access Memory
This is the major portion of memory in the Rabble 65. The computer can store values in distinct locations in RAM and recall them as required or alter them again. This type of memory is volatile, lost when power is removed.

Raw data
Information read from the disk, which includes timing references called clock pulses.

Return
To exit a subroutine and continue the programme from the point where the subroutine was called.

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RIOT
RAM I/O Timer. This is a chip used in the Rabble 65 which contains 128 bytes of RAM, sixteen lines of I/O in two ports, and a timer.

RS232
A standard to which serial I/O is transferred.

Run
An instruction contained in some high level languages to instruct the computer to start executing a programme.

SCan line
A single sweep of the cathode beam across the face of the CRT.

Scroll
To move all the text on the CRT up one text line to make room for more text.

Sector
A segment of a track on a disk.

Software
The programmes put into the computer to instruct the hardware what to do.

Stack
A reserved area in memory which is used to store information tempoarily. The data on a stack is not referenced by the address it occupies, but by the order in which it was placed on the stack. The last datum pushed onto the stack is the next one to be pulled from it.

Strobe
A short signal pulse which indicates that a specific event has occurred. The Rabble 65 uses a strobe to indicate to yhe parallel printer that a character has been placed on it's data buss.

Subroutine
A section of the programme in any level of language, which can be executed by a single instruction. Subroutines are used to conserve memory, where the same sequence of instructions are performed at many places throughout a programme.

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Syntax
: The grammatical arrangement of words or codes used to construct a programme. An syntactical error will produce an error message on the screen. For BASIC language the message is '?SN ERROR', for the extended monitor it is '?'.

Text
: Characters input or output to or from the computer. Text usually consists of alpha numeric data.

Timer
: A section of a VIA or RIOT or other hardware device which can indicate a predetermined interval of time.

Timing
: Relationship in time of the occurence of one event to another. The Rabble 65 uses the phase 2 clock as the reference to which all other events are related.

Track
: (1) A conductive path on the PCB along which electric current is passed. (2) A circular section of the disk on which data is stored. Disks can contain as many as 80 concentric tracks.

VIA
: Versatile Interface Adapter. Another type of I/O device. This device contains sixteen lines, in two ports, and timers. The timers are not implemented on the VIA used in the Rabble 65.

Video
: The signal presented to the monitor for display on the CRT.

Warm start
: To restart the operation of a programme without resetting all the initialisation routines.

Window
: An area of the CRT reserved for a specific application, under software control.

Zero page
: The first page of RAM in the Rabble 65 is called the zero page. It is used by the system operating software to temporarily store data and reference addresses.

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